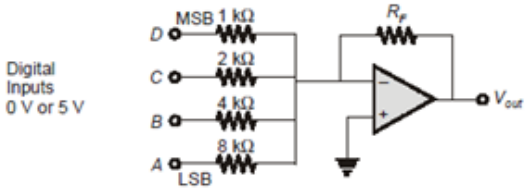
MSMF GATE CENTRE

DIGITAL CIRCUITS - 2

1. The step size of DAC in figure given below is 1 Volt



logic 0 – 0 V

logic 1 = 1 V

The value of R_F is

a) $1.5k\Omega$ b) $0.8k\Omega$ c) $8k\Omega$ d) $16k\Omega$

2. Which of the following statements is/are true.

(i) ECL RAMS are used as cache memory

(ii) Speed of MOSFET memory is larger as compared to BJT memory

(iii) In ROM random access is possible

a) i and ii b) ii and iii c) i and iii d) All of these

3. Which of the following statements is/are correct about Analog to Digital converters (ADCs)

(i) Flash type ADCs are fastest

(ii) In successive approximation type ADCs conversion time depends on magnitude of analog voltage.

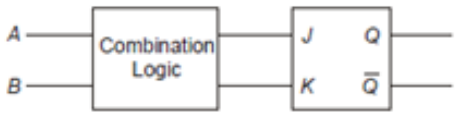
(iii) Counter type ADCs has fixed conversion time

(iv) Dual-slope type ADCs are slowest

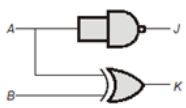
a) All of these b) ii and iii c) i and iv d) i only

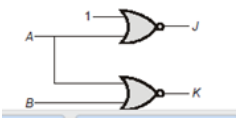
4. A new two input flip flop is designed as shown in figure. The table shows the characteristic table of the A – B flip flop

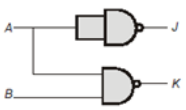
A	B	O_{n+1}
0	0	$\overline{O}_n$
0	1	1
1	0	O_n
1	1	0

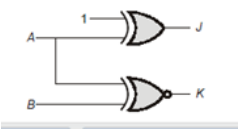


The combination logic is

a) 

b) 

c) 

d) 

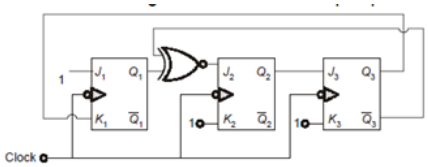
5. The minimum number of 2-input NAND gates required to implement the Boolean function.

$Y=(B+C)(\overline{A}+\overline{D})$ are _____

6. A finite state machine M, is constructed by connecting output of a 3-state, finite state machine inputs of a 9-state, finite state machine, M is reimplemented using a state register with the minimum number of bits. The minimum number of bits in state register is _____

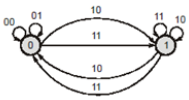
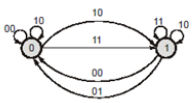
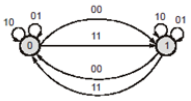
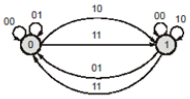
7. The ratio of maximum conversion time of 8 bit digital ramp type ADC to that of 8 bits successive approximation type is _____

8. Consider the circuit given below. If all the flip-flops are initially cleared then the count (Q_3 Q_2 Q_1)after 111 clock pulses is

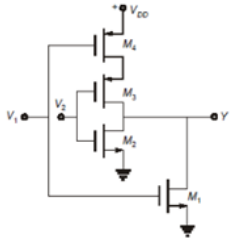


a) 000 b) 110 c) 101 d) 011

9. Identify the state diagram of J-K flip – flop. Here the first input (*J*) is represented by the MSB of input and the second input (*K*) is represented by the LSB of input.

a)  b)  c)  d) 

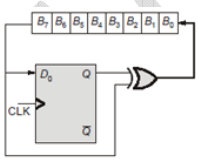
10. The CMOS circuit shown below represents



a) Positive logic NAND gate b) Positive logic NOR gate

c) Positive logic AND gate d) Positive logic OR gate

11. An 8-bit register and D flip flop shown in figure below are synchronized with same clock

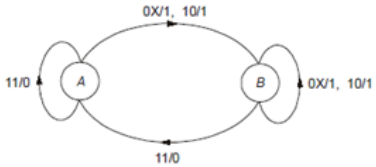


Assuming the flip flop is initially cleared. The circuit act as a

a) Binary to 2 s compliment converter b) Binary to Gray code converter

c) binary to 1's compliment converter d) Binary to Excess – 3 converter

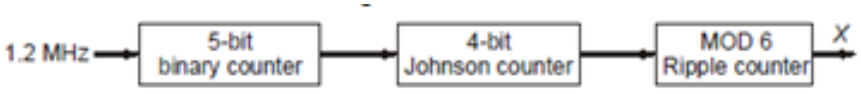
12. The state diagram of a Mealy circuit is shown in figure. Where "X" represents the don't care condition.



the circuit corresponding to the given state diagram can be used as _____

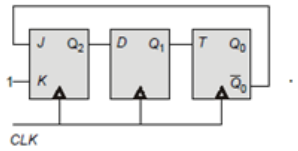
a) OR gate b) AND gate c) NOR gate d) NAND gate

13. Consider the counter stages shown below



The frequency at point X is _____ Hz.

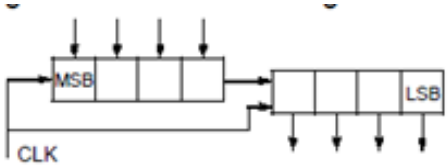
14. Consider the following synchronous counter made up of J-K, D and T Flip – Flops.



If the initial state $(Q_2\, Q_1\, Q_0)$ of the counter is 101, then the state (Q_2 Q_1 Q_0) after 4 clock pulses is _____

15. The number of clock pulses needed to change the contents of an 8-bit up counter from $(10101011)_2$ to $(00111010)_2$ is _____

16. An 8-bit register is made of one 4-bit PISO register [Synchronous loading] cascaded with a 4-bit SIPO register as shown in the figure below.



Total number of clock pulses required to perform write and read operations for one byte is _____

ANSWERS :

1.a	2.c	3.c	4.d	5.4	6. 5
7.32	8.c	9.d	10.b	11.b	12.d
13.781.25 (780.00 – 782.00)			14. 010	15. 143	16. 10