MSMF GATE CENTRE

Sub: MICROPROCESSORS

Time: 50min **Date:20-12-16** **Marks:33**

1. Which interrupt has highest priority in 8085 microprocessor ?
   a) INTR b) RST 4.5 c) RST 6.5 d) RST 7.5
2. In 8085 microprocessor, the 16 bit register(s) is/are
   a) Stack pointer b) Program counter c) Both (a) and (b) d) Accumulator
3. The contents of accumulator after execution of CMA instruction is A5 H. Its contents before execution is
   a) A5 H b) 5A H c) 55 H d) AA H
4. The serial input data of 8085 microprocessor can be loaded into MSB of the accumulator by
   a) executing RIM instruction b) executing RST1
   c) using TRAP d) none of these
5. The advantage(s) of memory mapped I/O over I/O mapped I/O is/are
   a) faster accessing
   b) more number of instructions supporting memory mapped I/O
   c) more number of I/O devices can be interfaced
   d) all of the above
6. Which of the following mainly decides the speed of operation of a microprocessor ?
   a) input clock frequency b) data bus width
   c) Address bus width d) all of the above
7. Which of the following Assembly language instruction can be used to clear the lower four bits of the accumulator in 8085 microprocessor ?
   a) XRI 0F H b) ANI F0 H c) XRI F0 H d) ANI 0F H
8. The size of ROM used to store the table for multiplication of two 8 bit unsigned integers must be
   a) 256 × 16 b) 64 k × 8 c) 4 k × 16 d) 64 k × 16
9. In 8085 microprocessor, if CMP B is executed and the status of carry flag and zero flag are set and reset respectively, then which of the following is true ?
   a) Contents of Accumulator is equal to that of register B
   b) Contents of Accumulator is greater than that of register B
   c) Contents of Accumulator is less than that of register B
   d) Such status of carry and zero flags is not possible, when CMP B is executed.
10. Consider the following set of Assembly language instructions of 8085 microprocessor
    STC
    CMC
    MOV A, B
    RAL
    MOV B, A
    The above set of instructions
    a) doubles the contents of Register B b) divides the contents of Register B by 2
    c) multiplies the contents of B by A d) Swaps the contents of Register A and B
11. In 8085 microprocessor, when RST n instruction is executed, the contents of program counter is 0018 H. The value of *n* is _____
    a) 3 b) 2 c) 6 d) 1

12. Consider the following Assembly Language program.

MVI A, 30 H

ADI 30 H

XRA A

POP H

After execution of the above program, the contents of Accumulator will be (_____) 10.

a) 3 b) 0 c) 6 d) 1

13. Let a memory chip is represented as 8192 × 64. If there are A number of address lines and B number of data lines in the chip, then A + B is _____

a) 77 b) 78 c) 80 d) 10

14. The number of machine cycles required to execute the instruction PUSH B is _____

a) 6 b) 4 c) 3 d) 2

15. The following set of instructions is executed by an 8085 microprocessor

100 H LXI SP, 27 FF H

1003 H CALL 1006 H

1006 H POP H

The contents of HL register pair after execution of above set of instructions is _____ H.

a) 1005 b) 1004 c) 100 d) 1006

16. The addressable memory capability supported by 8085 microprocessor is _____ kB.

a) 62 b) 64 c) 60 d) 56

17. How many times, the LOOP will be executed in the following assembly language program ?

LXI B, 0002 H

LOOP : DCX B

MOV A, C

XRA B

JNZ LOOP

HLT

a) once b) twice c) zero d) infinite

18. The 'DMA' transfer implies

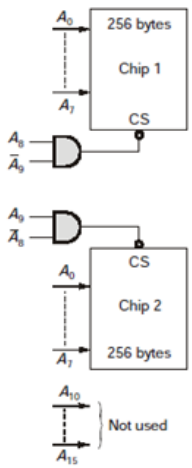
a) direct transfer of data between memory and accumulator

b) direct transfer of data between memory and I/O devices without the interference of microprocessor.

c) transfer of data exclusively within microprocessor registers.

d) A fast transfer of data between microprocessor and I/O devices.

19. Consider the following memory interfacing diagram with 8085 microprocessor.



What memory address range in the given options is NOT represented by combination of chip 1 and chip 2? (A_0 to A_{15} are address lines and CS means chip select)

a) 0100 H – 02FF H b) F900H – FAFF H c) 1500 H – 16FF H d) F800 H – F9FF H

20. Consider an 8085 microprocessor system. The following program starts at location 0700 H.

```
LXI SP, 00FF H
LXI H, 0701 H
MVI A, 20 H
SUB M
```

The contents of accumulator when the program counter reaches 0709 H is

a) 00 H b) 21 H c) 20 H d) FF H

21. Consider the following set of instructions to be executed by an 8085 microprocessor. The input port having an address of 01 H has the data 05 H.

```
IN 01 H
ANI 80 H
```

After execution of the above two instructions, the contents of flag register will be

	D7	D6	D5	D4	D3	D2	D1	D0
(a)	1	0	x	1	x	1	x	0
(b)	0	1	x	0	x	1	x	0
(c)	0	1	x	1	x	1	x	0
(d)	0	1	x	1	x	0	x	0

a) a b) b c) c d) d

22. Consider the following statements

(i) DAD Rp doesn't affect any flag.

(ii) PCHL exchanges the content of program counter and HL pair.

(iii) PUSH Rp, INX Rp, PCHL, SPHL and XTHL, all these instruction have opcode fetch of 6-Tstates.

(iv) In INR R, all flags are affected except CY flag.

(Rp : Register pair and R : Register)

Which of the above statements are NOT correct ?

a) I and iv b) ii, iii and iv c) I, ii, iii and iv d) I, ii and iii

23. When RET instruction at the end of subroutine is executed,

a) the information where the stack is initialized is transferred to the stack pointer

b) the memory address of RET instruction is transferred to the program counter

c) the two data bytes stored in the top two locations of the stack are transferred to the program counter.

d) the two data bytes stored in the top two locations of the stack are transferred to the stack pointer.

24. Match List – I (Instruction) with List – II (Operation) for intel 8085 microprocessor and select the correct answer using the codes given below :

List – I	List – II
A. PCHL	1. Exchange the top of the stack with contents of HL pair
B. SPHL	2. Exchange the contents of HL pair with that of DE pair
C. XTHL	3. Transfer the contents of HL pair to the stack pointer
D. XCHG	4. Transfer the contents of HL pair to the program counter

Codes

	A	B	C	D		A	B	C	D
a)	3	4	1	2	b)	3	4	2	1
c)	4	3	2	1	d)	4	3	1	2

25. After execution of the following set of instructions of 8085 microprocessor, the contents of Accumulator will be

3000 H : MVI A, 45 H
3002 H : MOV B, A
3003 H : STC
3004 H : CMC
3005 H : RAR
3006 H : XRA B
3007 H : HLT

a) 00 H b) 45 H c) 67 H d) E7 H

26. Consider the following set of instructions

MVI A, BYTE 1
RLC
MOV B, A
RLC
RLC
ADD B

If the contents of Accumulator, after the execution of the program is 46 H, then the contents of BYTE 1 Initially will be

a) 06 H b) 07 H c) 08 H d) 09 H

27. The following set of instructions is executed in an 8085 microprocessor based system. The frequency of clock of microprocessor is 5 MHz.

	T – states
XRA A	4T
LXI SP, 3A00H	10T
LXI H, 0000H	10T
LOOP : DADSP	10T
SHLD 4000H	16T
JC LOOP	7T/10T
NOP	4T

The total time required to execute the above set of instruction is _____ µsec

a) 12.2 b) 13.4 c) 14.2 d) 10.2

28. The minimum number of memory IC's of 4 k × 2 capacity required to construct a memory of 22 k × 8 capacity is _____

a) 26 b) 24 c) 26 d) 12

29. An INTEL 8085 microprocessor is interfaced with a memory chip of unknown size. The starting address by which memory can be addressed is 1001 H and the ending address is 2016 H. The size of the memory chip is _____ bytes.

a) 4118 b) 4110 c) 4222 d) 4000

30. If the time required to execute JMP 2017 H instruction is 2.5 microseconds, the the crystal frequency of 8085 microprocessor is _____ MHz.

a) 8 b) 2 c) 6 d) 1

31. A memory system of 64 K bytes needed to be designed with RAM chips of 1K byte each and a decoder tree constructed with 2 : 4 decoder chips with 'enable' input. The total number of decoder chips required is _____

a) 22 b) 24 c) 26 d) 21

32. The contents of some memory locations of an 8085 microprocessor based system are given as follows.

Address	Contents
3000 H	02 H
3001 H	30 H
3002 H	00 H
3003 H	30 H

Consider the assembly language program given below

```
LXIH, 3000 H
MOV E, M
INX H
MOV D, M
LDAXD
MOV L, A
INX D
LDAXD
MOV H, A
NOP
```

The contents of register H after execution of the above program will be (_____)10.

a) 32 b) 24 c) 48 d) 28

33. Consider the assembly language program given below

```
XRA A
STA E008 H
DCR a
STA A008 H
HLT
```

The contents of memory location A008H after execution of the above program in 8085 microprocessor is (_____)10.

a) 256 b) 255 c) 65 d) 125

Answers :

1.b	2.c	3.b	4.a	5.d	6.a	7.b	8.d	9.c	10.a	11.a	12.b	13.a	14.c
15. d	16. b		17.b	18.b	19.d	20.b	21.c	22.d	23.c	24.d	25.c	26.b	
27. a		28. b		29. a	30. a		31. D	32. c		33. b			