UNIT-I

SEMICONDUCTOR DEVICES

SEMICONDUCTOR MATERIALS:

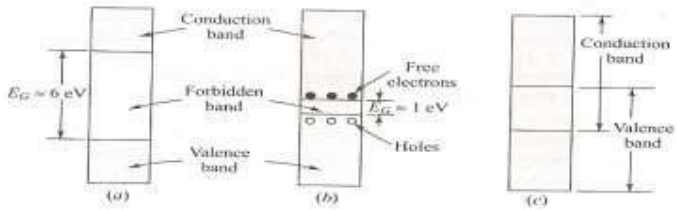


Fig.1 *Energy-band structure of (a) an insulator, (b) a semiconductor, and (c) a metal.*

INSULATOR:

An insulator is a material that offers a very low level of conductivity under Pressure from an applied voltage source. In this material Forbidden energy gap is large (EG6e.V). So, electron cannot acquire enough energy and hence conduction is not possible .Ex: Diamond is a perfect insulator.

SEMI CONDUCTOR:

A semiconductor is a material that has a conductivity level somewhere in between the extremes of an insulator and a conductor. Energy gap is only about 1ev. Ex: Germanium, Silicon (Energy gap of Germanium is about 0.785ev and for silicon it s 1.21ev).

CONDUCTOR:

Conductor is a material that will support a generous flow of charge when a voltage source of limited magnitude is applied across its terminals. There is no energy gap in conductors. Conduction band and valence band are overlapped. Ex: Copper, Aluminum.

DOPING:

Adding impurities to the semiconductor is known as doping. Pure semiconductor is called as intrinsic semiconductor & impure semiconductor is called extrinsic semiconductor materials.

EXTRINSIC MATERIALS-*n* and *p*-type:

The characteristics of semiconductor materials can be altered significantly by the addition of certain impurity atoms into the relatively pure semiconductor material .These impurities, although only added to perhaps 1partin10million,can alter the band structure sufficiently to totally change the electrical properties of the material. A semiconductor material that has been subjected to the doping process is called an extrinsic material. There are two extrinsic materials of immeasurable importance to semiconductor device fabrication: *n*-type and *p*-type.

N-Type Material:

Both the *n*-and *p* type materials are formed by adding a predetermined number of impurity atoms in to a germanium or silicon base. The *n*-type is created by introducing those impurity elements that have five valence electrons (pentavalent), such as antimony, arsenic, and phosphorus. The effect of such impurity elements is indicated in

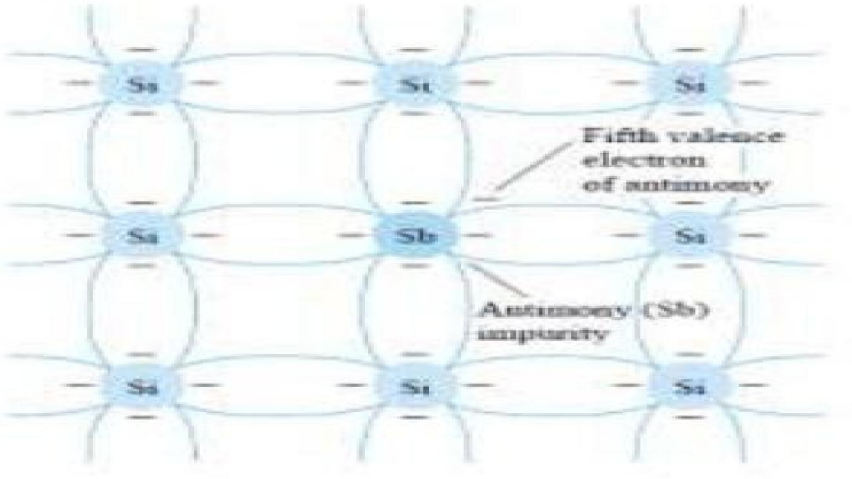


Figure.1 Antimony impurity in n-type material

Fig.1 (using antimony as the impurity in a silicon base). Note that the four covalent bonds are still present. There is, however, an additional fifth electron due to the impurity atom, which is *unassociated* with any particular covalent bond. This remaining electron, loosely bound to its parent (antimony) atom, is relatively free to move within the newly formed *n*-type material. Since the inserted impurity atom has donated a relatively free electron to the structure: Diffused impurities with five valence electrons are called donor atoms**.**

P-Type Material:

The p-type material is formed by doping a pure germanium or silicon crystal with impurity atoms having three valence electrons. The elements most frequently used for this purpose are boron, gallium, and indium. The effect of one of these elements, boron, on a base of silicon.

Note that there are now an insufficient number of electrons to complete the covalent bonds of the newly formed lattice. The resulting vacancy is called a *hole* and is represented by a small circle or positive sign due to the absence of a negative charge. Since the resulting vacancy will readily. *Accept* a free electron: The diffuse impurities with three valence electrons are called acceptor atoms.

Majority and Minority Carriers:

In the intrinsic state, the number of free electrons in Ge or Si is due only to those few electrons in the valence bands that have acquired sufficient energy from thermal or light sources to break the covalent bond or to the few impurities that could not be removed. The vacancies left behind in the covalent bonding structure represent our very limited supply of holes. In an *n*-type material, the number of holes as not changed significantly from this intrinsic level. Then result, therefore, is that the number of electrons far outweighs the number of holes. In an n-type material the electron is called the majority carrier and the hole the minority carrier .For the *p*-type material the number of holes far outweighs the

number of electrons ,as shown in Fig.1.13b. Therefore: In a p-type material the hole is the majority carrier and the electron is the minority carrier. When the fifth electron of a donor atom leaves the parent atom, the atom remaining acquires a positive charge: hence the positive sign in the donor-ion representation.

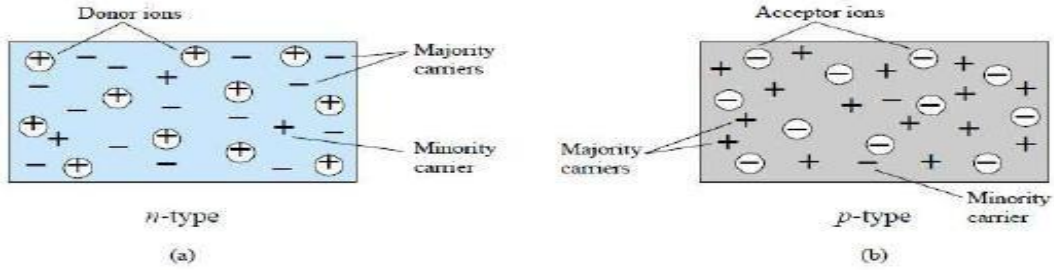


Figure 1.13 (a) *n*-type material; (b) *p*-type material.

Fermi Level in N & P type materials is shown in below Fig:

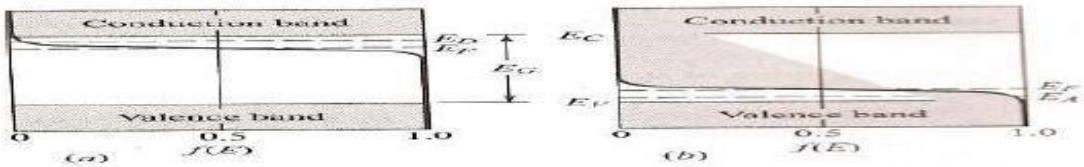


Fig. Positions of Fermi level in (a) n-type and (b) p-type semiconductors.

In N type material Fermi level is just below the conduction band. In P type material Fermi level is just above the valence band.

BAISING OF PN DIODE:

The semiconductor diode is formed by simply bringing these materials together (constructed from the same base Ge or Si), as shown in Fig. At the instant the two materials are joined the electrons and holes in the region of the junction will combine, resulting in a lack of carriers in the region near the junction. This region of uncovered positive and negative ions is called the depletion region due to the depletion of carriers in this region. Since the diode is a two-terminal device, the application of a voltage across its terminals leaves three possibilities: *no bias* (*VD* = 0 V), *forward bias* (*VD* >0 V), and *reverse bias* (*VD*< 0 V).No Applied Bias (*VD* = 0 V) under no-bias (no applied voltage) conditions, any minority carriers (holes) in the *n*-type material that find themselves within the depletion region will pass directly into the *p*-type material. The closer the minority carrier is to the junction, the greater the attraction for the layer of negative ions and the less the opposition of the positive ions in the depletion region of the n type material. For the purposes of future discussions we shall assume that all the minority carriers of the *n*-type material that find themselves in the depletion region due to their random motion will pass directly into the *p*-type material. Similar discussion can be applied to the minority carriers (electrons) of the *p*-type material.

This carrier flow has been indicated in fig for the minority carriers of each material. The majority carriers (electrons) of the *n*-type material must overcome the attractive forces of the layer of positive ions in the *n*-type material and the shield of negative ions in the *p*-type material to migrate into the area beyond the depletion region of the *p*-type material. However, the number of majority carriers is so large in the *n*-type material that there will invariably be a small number of majority carriers with sufficient kinetic energy to pass through the depletion region into the *p*-type material. Again, the same type of discussion can be applied to the majority carriers (holes) of the p-type material. The resulting flow due to the majority carriers is also shown in Fig. 1.14. In the absence of an applied bias voltage, the net flow of charge in any one direction for a semiconductor diode is zero. The symbol for a diode is repeated in Fig. with the associated *n*- and *p*-type regions. Note that the arrow is

associated with the *p*-type component and the bar with the *n*-type region. As indicated, for *VD*= 0 V, the current in any direction is 0 mA.

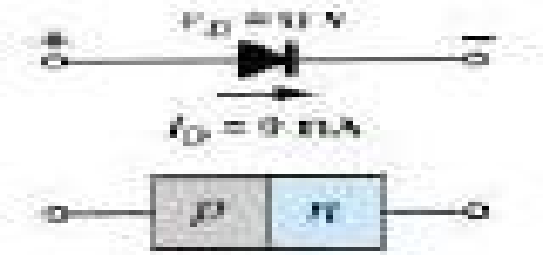


Figure: No-bias conditions for a semiconductor diode.

Reverse-Bias Condition (*VD* < 0 V): The external potential is connected such that n-type material is connected to positive terminal and p-type is connected to negative terminal of the battery. As shown in Fig. 1.16, the number of uncovered positive ions in the depletion region of the *n*- type material will increase due to the large number of free electrons drawn to the positive potential of the applied voltage. For similar reasons, the number of uncovered negative ions will increase in the *p*-type material. The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero as shown in Fig.

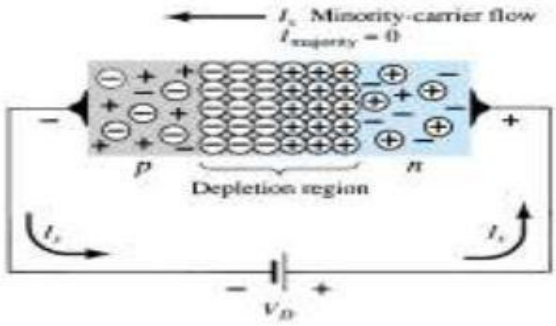


Figure 1.16 Reverse-biased p-n junction.

The number of minority carriers, however, that find themselves entering the depletion region will not change, resulting in minority-carrier flow vectors of the same magnitude. With no applied voltage the current that exists under reverse-bias conditions is called the reverse saturation current and is represented by I_o.

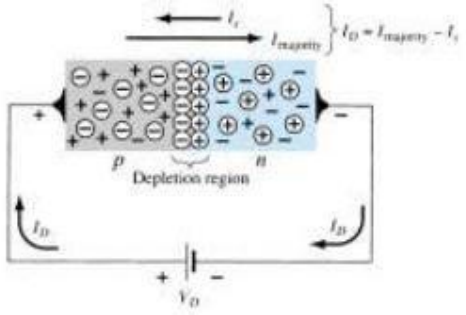


Figure1.18 Forward-biased *p-n junction*

ZENER DIODES:

The characteristic drops in an almost vertical manner at a reverse-bias potential denoted V_Z.The fact that the curve drops down and away from the horizontal axis rather than up and away for the positive V_D region reveals that the current in the Zener region has a direction opposite to that of a forward-biased diode.

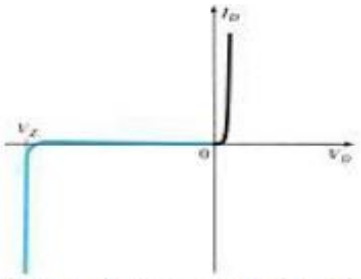


Fig.1.47 zener diode characteristics

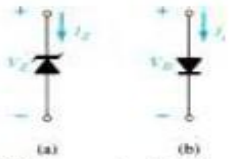
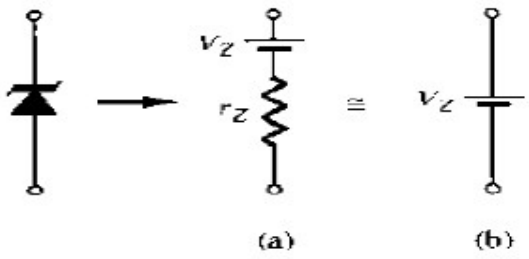


Figure 1.48 Conduction direction:
(a) Zener diode; (b) semiconductor diode

This region of unique characteristics is employed in the design of Zener diodes, which have the graphic symbol appearing in Fig. 1.48a. Both the semiconductor diode and Zener diode are presented side by side in Fig. 1.48 to ensure that the direction of conduction of each is clearly understood together with the required polarity of the applied voltage. For the semiconductor diode the —on state will support a current in the direction of the arrow in the symbol. The location of the Zener region can be controlled by varying the doping levels. An increase in doping, producing an increase in the number of added impurities, will decrease the Zener potential. Zener diodes are available having Zener potentials of 1.8 to 200 V with power ratings from 14 to 50 W. Because of its higher temperature and current capability, silicon is usually preferred in the manufacture of Zener diodes.



The complete equivalent circuit of the Zener diode in the Zener region includes a small dynamic resistance and dc battery equal to the Zener potential, as showninFig.1.49.

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RECTIFIERS & FILTERS:

For the operation of most of the electronics devices and circuits, a d.c. source is required. So it is advantageous to convert domestic a.c. supply into d.c. voltages. The process of converting a.c. Voltage into d.c. voltage is called as rectification. This is achieved with

i) Step-down Transformer, ii) Rectifier, iii) Filter and iv) Voltage regulator circuits.

These elements constitute d.c. regulated power supply shown in the figure below. The block diagram of a regulated D.C. power supply consists of step-down transformer, rectifier, filter, voltage regulator and load. An ideal regulated power supply is an electronics circuit designed to provide a predetermined d.c. voltage Vo which is independent of the load current and variations in the input voltage ad temperature. If the output of a regulator circuit is a AC voltage then it is termed as voltage stabilizer, whereas if the output is a DC voltage then it is termed as voltage regulator.

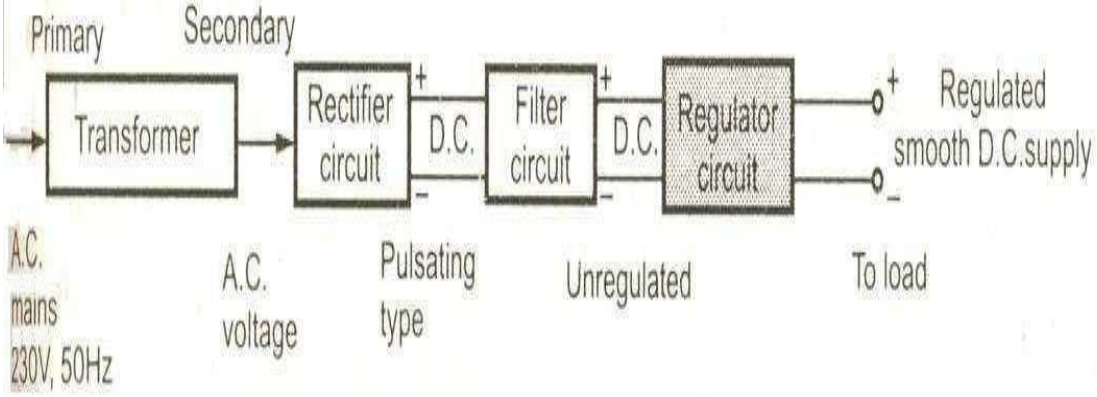
The elements of the regulated DC power supply are discussed as follows:

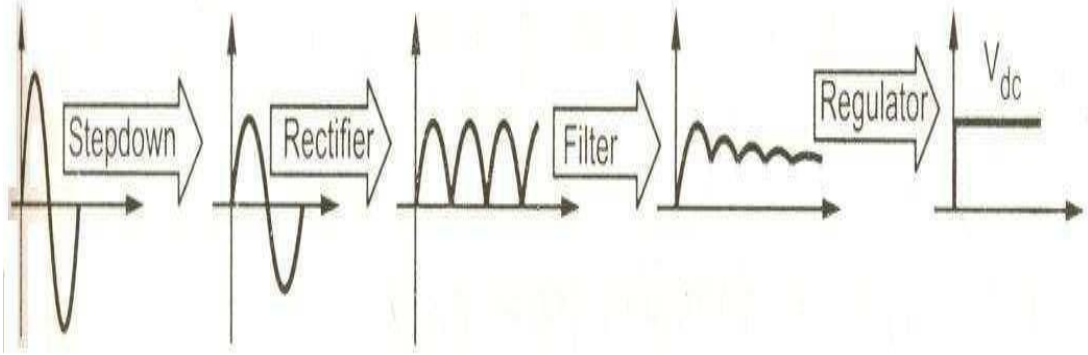
TRANSFORMER:

A transformer is a static device which transfers the energy from primary winding to secondary winding through the mutual induction principle, without changing the frequency.

The transformer winding to which the supply source is connected is called the primary, while the winding connected to the load is called secondary. The different types of the transformers are

1. Step up transformer 2. Step down transformer





RECTIFIER:

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional waveform, with a non-zero average component. A rectifier is a device which converts a.c. voltage (bi-directional) to pulsating d.c. voltage (Uni-directional).

Important characteristics of a Rectifier Circuit:

1. **Load currents:** They are two types of output current. They are average or d.c. current and RMS currents.

Average or DC current: The average current of a periodic function is defined as the area of one cycle of the curve divided by the base. It is expressed as

$$I_{dc} = 1/2\pi \int_0^{2\pi} id(\omega t) \text{ ; where } i = \mathrm{I}_m \sin \omega t$$

Effective (or) R.M.S. current: The effective (or) R.M.S. current squared of a periodic function of time is given by the area of one cycle of the curve which represents the square of the function divided by the base. It is expressed as

$$\mathbf{I}_{\text{rms}} = 1/2\pi \int_0^{2\pi} i2 \, d\omega t$$

Average or DC Voltage: The average voltage of a periodic function is defined as the areas of one cycle of the curve divided by the base.

$$V_{dc} = I_{dc} \times R_L$$

2. **Effective (or) R.M.S Voltage:** The effective (or) R.M.S voltage squared of a periodic function of time is given by the area of one cycle of the curve which represents the square of the function divided by base.

$$V_{rms} = I_{rms} \times R$$

3. **Ripple Factor** (γ) **:** It is defined as ration of R.M.S. value of a.c. component to the d.c. Component in the output is known as "Ripple Factor".

$$\gamma = Vrms/V_{dc}$$

4. **Efficiency** (η) **:** It is the ratio of d.c output power to the a.c. input power. It signifies, how efficiently the rectifier circuit converts a.c. power into d.c. power. It is given by

$$\eta = \mathrm{P}_{dc/} P_{ac}$$

5. **Peak Inverse Voltage (PIV):** It is defined as the maximum reverse voltage that a Diode can withstand without destroying the junction.

6. **Regulation:** The variation of the d.c. output voltage as a function of d.c. load current is called regulation.

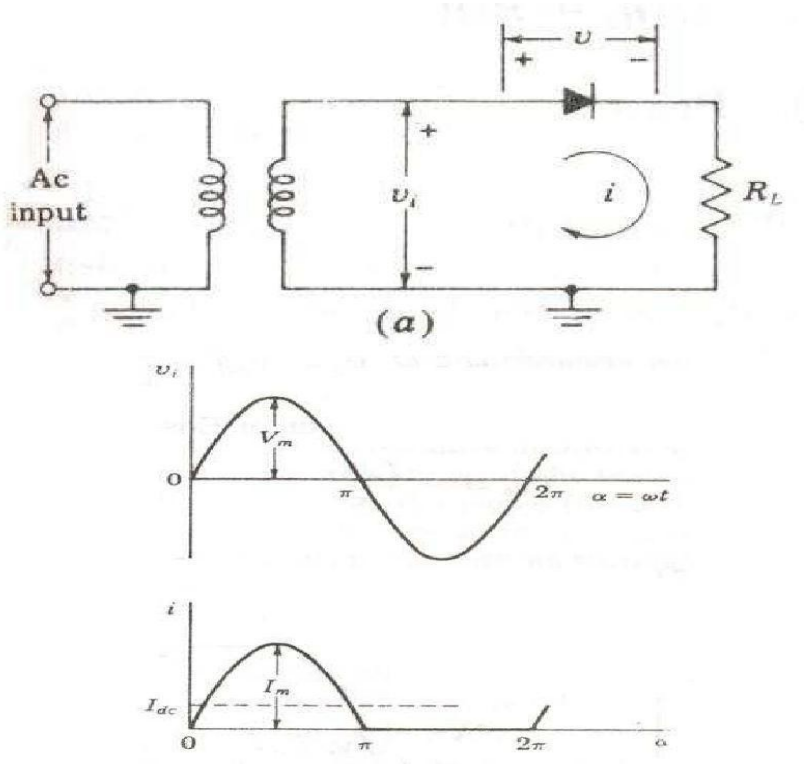
$$\%\text{Regulation} = (v_{nl}-v_{fl})/v_{fl}*100$$

For an ideal power supply, % Regulation is zero.

Using one or more diodes in the circuit, following rectifier circuits can be designed.

1. Half-Wave Rectifier
2. Full –Wave Rectifier
3. Bridge Rectifier

Half wave rectifier: A Half – wave rectifier is one which converts a.c. voltage into a pulsating voltage using only one half cycle of the applied a.c. voltage. The basic half-wave diode rectifier circuit along with its input and output waveforms.



The half-wave rectifier circuit shown in above figure consists of a resistive load; a rectifying element i.e., p-n junction diode and the source of a.c. voltage, all connected is series. The a.c. voltage is applied to the rectifier circuit using step-down transformer. The input to the rectifier circuit, $V = V_m \sin \omega t$ Where V_m is the peak value of secondary a.c. voltage.

Operation: For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across R_L. The waveform of the diode current (or) load current is shown in figure. For the negative half-cycle of input, the diode D is reverse biased and hence it does not conduct. Now no current flows in the circuit i.e., i=0 and Vo=0. Thus for the negative half-cycle no power is delivered to the load.

Analysis: In the analysis of a HWR, the following parameters are to be analyzed.

1. DC output current
2. DC Output voltage
3. R.M.S. Current
4. R.M.S. voltage

5. Rectifier Efficiency (η)
6. Ripple factor (γ)
7. Regulation
8. Transformer utilization factor (TUF)
9. Peak inverse voltage (PIV)

$V_{dc}=0.318I_m$

$I_{dc}=0.318V_m/R_L$

$I_{rms}=V_m/2(R_f+R_L)$

$V_{rms}=V_m/2$

$\eta=$ 40.6%

$\gamma=1.21$

TUF $=0.287$

Disadvantages of Half-Wave Rectifier:

1. The ripple factor is high.
2. The efficiency is low.
3. The Transformer Utilization factor is low.

Because of all these disadvantages, the half-wave rectifier circuit is normally not used as a power rectifier circuit.

FULL WAVERECTIFIER: A full-wave rectifier converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. In order to rectify both the half cycles of ac input, two diodes are used in this circuit. The diodes feed a common load R_L with the help of a center-tap transformer. A center-tap transformer is the one which produces two sinusoidal waveforms of same magnitude and frequency but out of phase with respect to the ground in the secondary winding of the transformer. The full wave rectifier is shown in the figure below.

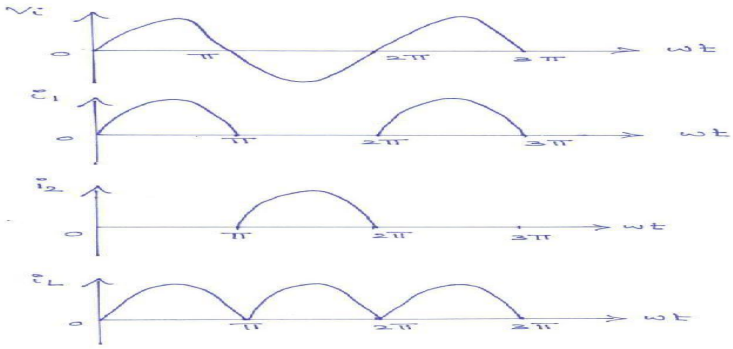
Operation: During positive half of the input signal, anode of diode D_1 becomes positive and at the same time the anode of diode D_2 becomes negative. Hence D_1 conducts and D_2 does not conduct. The load current flows through D_1 and the voltage drop across R_L will be equal to the input voltage.

During the negative half cycle of the input, the anode of D_1 becomes negative and the anode of D_2 becomes positive. Hence, D_1 does not conduct and D_2 conducts. The load current flows through D_2 and the voltage drop across R_L will be equal to the input voltage.

It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

1. $V_{dc}= 2V_m/\pi$
2. $I_{dc}=2I_m/\pi$
3. $\gamma = 0.48$
4. $\eta=$ 80%

5. TUF=o.812%



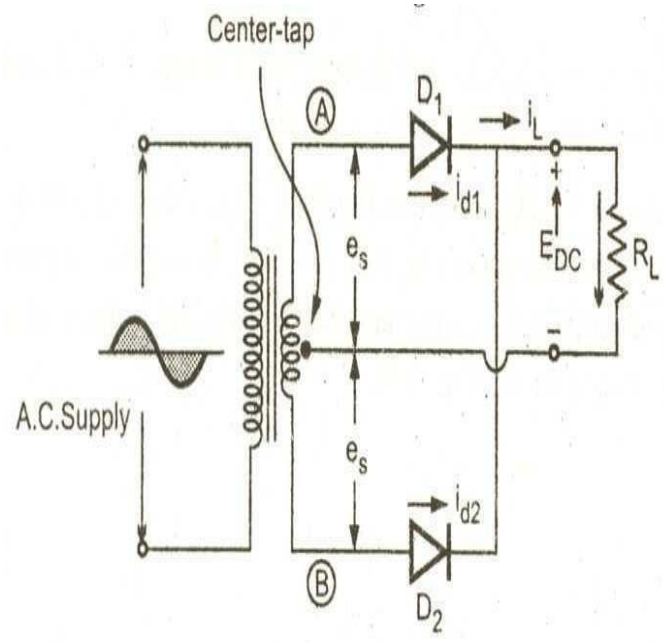
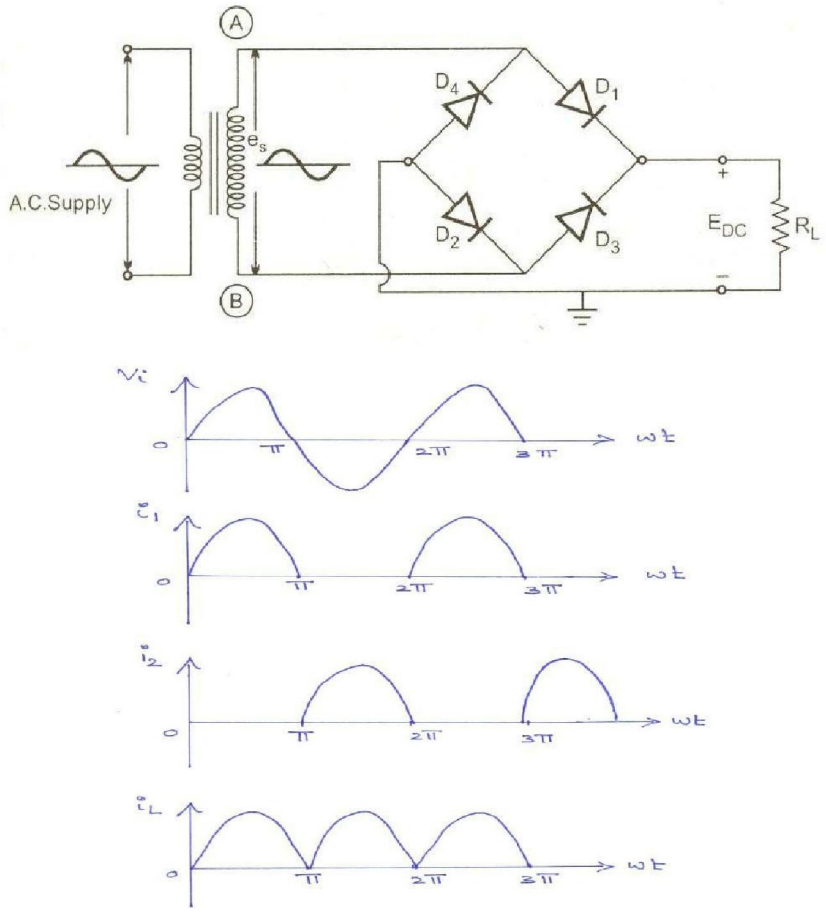


Fig. Full-Wave Rectifier

Bridge rectifier: The full wave rectifier circuit consists of a center tap transformer. But for a bridge rectifier the center tap is not required. The bridge rectifier consists of four diodes connected in the form of bridge. The ac input voltage is applied to diagonally opposite end so the bridge. The load resistance is connected between the other two ends of the bridge. The bridge rectifier circuits and its waveforms are shown in figure.



Operation: For the positive half cycle of the input ac voltage diodes D_1 and D_3 conduct, whereas diodes D_2 and D_4 do not conduct. The conducting diodes will be in series through the load resistance R_L, so the load current flows through the R_L.

During the negative half cycle of the input ac voltage diodes D_2 and D_4 conduct, Whereas diodes D_1 and D_3 do not conduct. The conducting diodes D_2 and D_4 will be in series through the load resistance R_L and the current flows through the R_L, in the same direction as in the previous half cycle. Thus a bidirectional wave is converted into a unidirectional wave.

Analysis: The average values of output voltage and load current, the rms values of voltage and current, the ripple factor and rectifier efficiency are the same as for as center tapped full-wave rectifier.

Advantages of Bridge rectifier circuit:

1) No center-tapped transformer is required.
2) The TUF is considerably high.
3) PIV is reduced across the diode.

Disadvantages of Bridge rectifier circuit:

The only disadvantage of bridge rectifier is the use of four diodes as compared to two diodes for center-tapped FWR. This reduces the output voltage.

FILTERS: The output of a half-wave (or) full-wave rectifier circuit is not pure d.c., but it contains fluctuations (or) ripple, which are undesired. To minimize the ripple content in the output, filter circuits are used. These circuits are connected between the rectifier and load. Ideally, the output of the filter should be pure d.c. practically, the filter circuit will try to minimize the ripple at the output, as far as possible. Basically, the ripple is ac, i.e., varying with time, while dc is a constant w.r.t. time.

Hence in order to separate dc from ripple, the filter circuit should use components which have widely different impedance for ac and dc. Two such components are inductance and capacitance. Ideally, the inductance acts as a short circuit for dc, but it has large impedance for ac.

Similarly, the capacitor acts as open for dc if the value of capacitance is sufficiently large enough. Hence, in a filter circuit, the inductance is always connected in series with the load, and the capacitance is connected in parallel to the load.

Definition of a Filter:

Filter is an electronic circuit composed of a capacitor, inductor (or) combination of both and connected between the rectifier and the load so as to convert pulsating dc to pure dc.

The different types of filters are:

1) Inductor Filter,
2) Capacitor Filter,
3) LC (or) L-Section Filter, and
4) CLC (or) ∏-section Filter.

Inductor Filter:

Half-Wave rectifier with series Inductor Filter:

The Inductor filter for half-wave rectifier is shown in figure below.

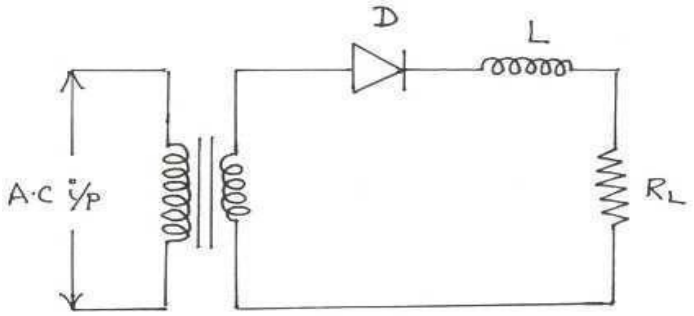


Fig: series inductor filter with HWR

In this the inductor is connected in series with the load. The inductor operation filter depends upon the property of the inductance to oppose any change of current that may flow through it. The ripple factor for the inductor HWR filter is $\gamma=1.13R_L/\omega_L$

Full-wave rectifier with series inductor filter:

A FWR with series inductor filter is shown in figure.

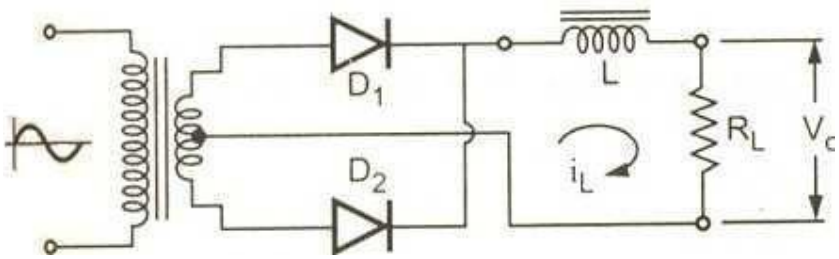


FIG: FWR with series inductor filter.

The inductor offers high impedance to a.c variations. The inductor blocks the a.c component and allows only the dc component to reach the load.

Half-wave rectifier with capacitor filter:

The half-wave rectifier with capacitor input filter is shown in figure below:

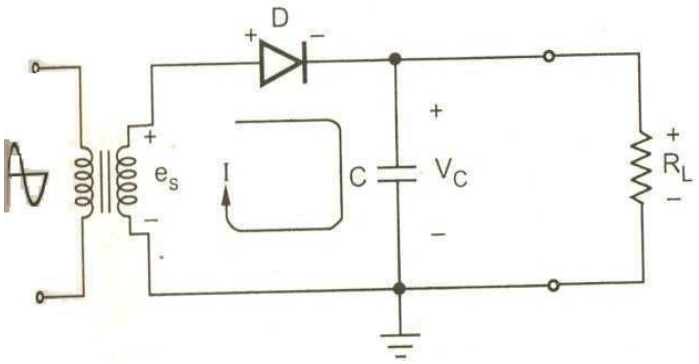


Fig: HWR with capacitor filter.

The filter uses a single capacitor connected in parallel with the load R_L. In order to minimize the ripple in the output, the capacitor C used in the filter circuit is quite large of the order of tens of microfarads.

The operation of the capacitor filter depends upon the fact that the capacitor stores energy during the conduction period and delivers this energy to the load during non-conduction period.

Operation:

During, the positive quarter cycle of the ac input signal, the diode D is forward biased and hence it conducts. This quickly charges the capacitor C to peak value of input voltage V_m. Practically the capacitor charge (V_m-Vγ) due to diode forward voltage drop.

When the input starts decreasing below its peak value, the capacitor remains charged at V_m and the ideal diode gets reverse biased. This is because the capacitor voltage which is cathode voltage of diode becomes more positive than anode.

Therefore, during the entire negative half cycle and some part of the next positive half cycle, capacitor discharges through R_L. The discharging of capacitor is decided by R_LC, time constant which is very large and hence the capacitor discharge very little from V_m.

In the next positive half cycle, when the input signal becomes more than the capacitor voltage, he diode becomes forward biased and charges the capacitor C back to V_m. The output waveform is shown in figure below:

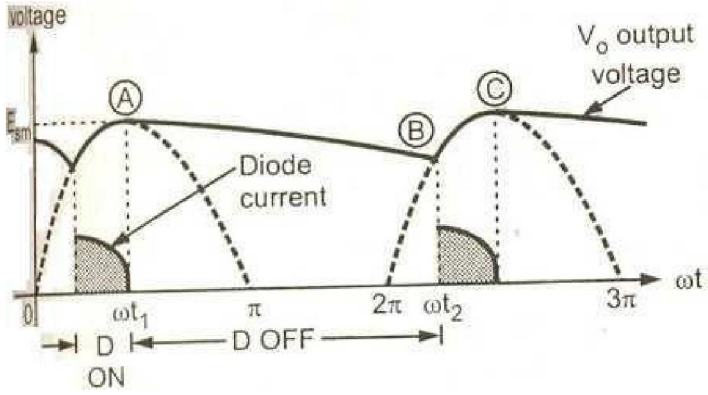


Fig: HWR output with capacitor filter.

Full-wave rectifier with capacitor filter:

The full-wave rectifier with capacitor filter is shown in the figure below:

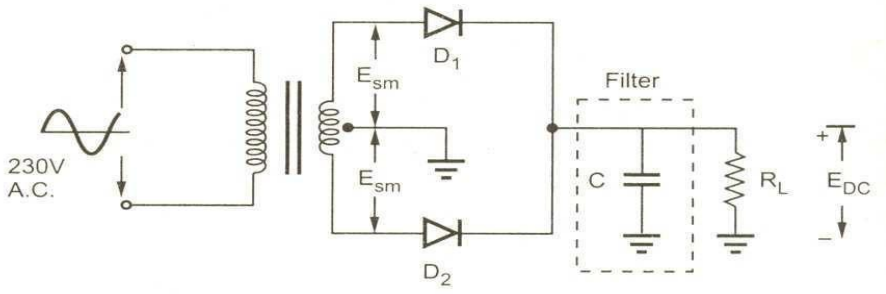
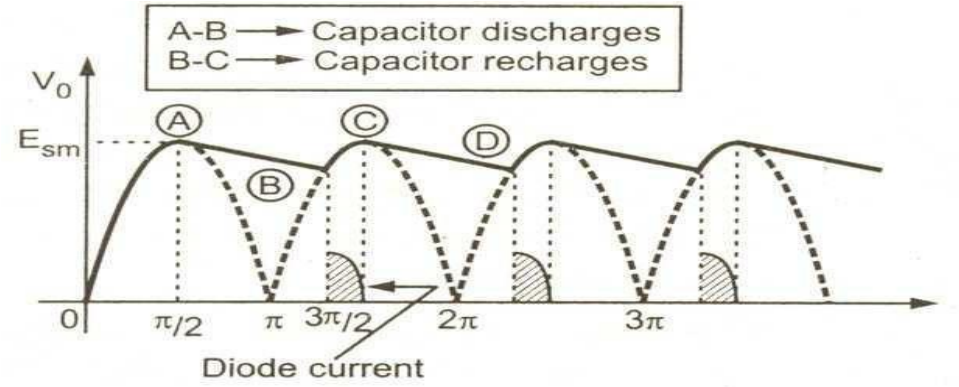


Fig: Full wave rectifier with capacitor filter

Operation:

During the positive quarter cycle of the ac input signal, the diode D_1 is forward biased the capacitor C gets charges through forward bias diode D_1 to the peak value of input voltage V_m. In FWR, as the time required by the capacitor to charge is very small and it discharges very little due to large time constant, hence ripple in the output gets reduced considerably. The output waveform is shown in figure below:



Full wave L Section Filter:

The series inductor filter and shunt capacitor filter are not much efficient to provide low ripple at all loads. The capacitor filter has low ripple at heavy loads while inductor filters at small loads. A combination of these two filters may be selected to make the ripple independent of load resistance. The resulting filter is called L-Section filter (or) LC filter (or) Choke input filter. This name is due to the fact that the inductor and capacitor are connected as an inverted L. A full-wave rectifier with choke input filter is shown in figure below:

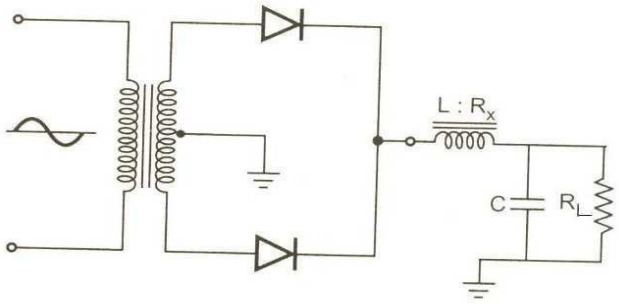


Fig: Full-wave rectifier with choke input filter.

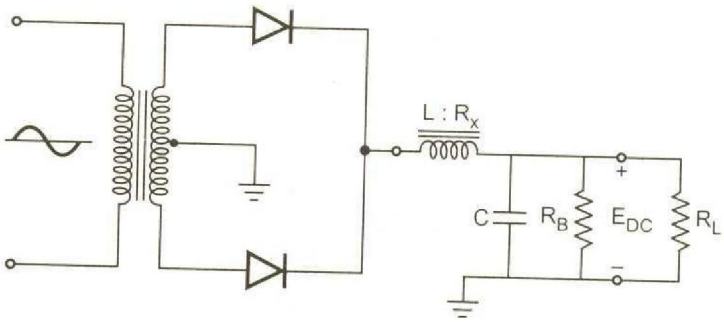
The action of choke input filter is like a low pass filter. The capacitor shunting the load bypasses the harmonic currents because it offers very low reactance to a.c. ripple current while it appears as an open circuit to dc current.

On the other hand the inductor offers high impedance to the harmonic terms. In this way, most of the ripple voltage is eliminated from the load voltage.

The necessity of Bleeder Resistance R_B:

The basic requirement of this filter circuit is that the current through the choke must be continuous and not interrupted. An interrupted current through the choke may develop a large back e.m.f which may be in excess of PIV rating of the diodes and/or maximum voltage rating of the capacitor C. Thus this back e.m.f is harmful to the diodes and capacitor. To eliminate the back e.m.f. developed across the choke, the current through it must be maintained continuous. This is assured by connecting a bleeder resistance, R_B across the output terminals.

The full-wave rectifier with LC filter and bleeder resistance is shown in the figure below:



Multiple L-Section filters:

The number of L-sections i.e., LC circuits can be connected one after another to obtain multiple L-section filter. It gives excellent filtering and smooth dc output voltage. The figure below shows multiple L-section filters.

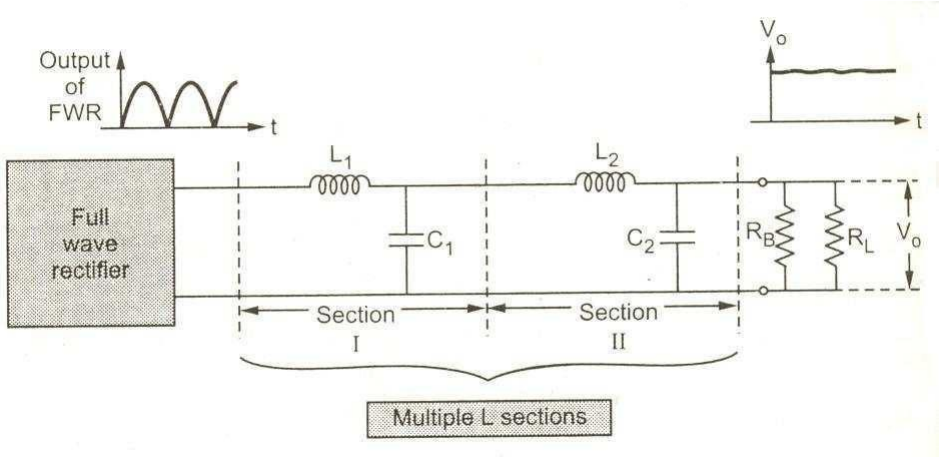


Fig: Multiple L-sections.

CLC Filter or π section filter:

This is capacitor input filter followed by a L-section filter. The ripple rejection capability of a Π-section filter is very good. The full-wave rectifier with Π-section filter is shown in the figure.

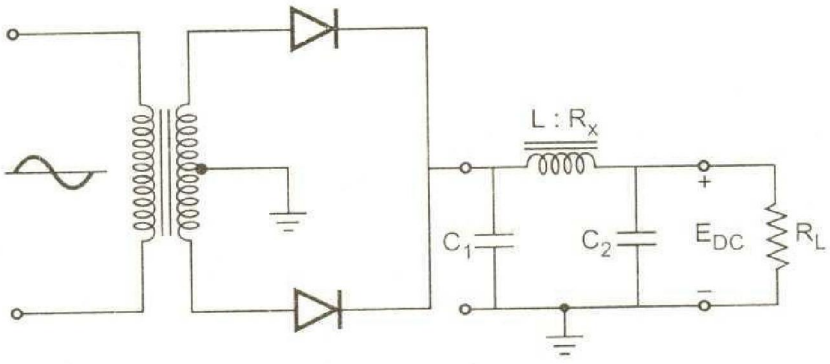


Fig: Π-section Filter.

It consists of an inductance L with a dc winding resistance as R_C and two capacitors C_1 and C_2. The filter circuit is fed from fill wave rectifier. Generally two capacitors are selected equal.

The rectifier output is given to the capacitor c_1. This capacitor offers very low reactance to the ac component but blocks dc component. Hence capacitor C_1 bypasses most of the ac component. The dc component then reaches to the choke L. The choke L offers very high reactance to dc. So it blocks ac component and does not allow it to reach to load while it allows dc component to pass through it. The capacitor C_2 now allows passing remaining ac component and almost pure dc component reaches to the load. The circuit looks like a Π, hence called Π-Filter.

UNIT-II

BJT and FETs

The transistor was invented in 1947 by John Bardeen, Walter Brattain and William Shockley at Bell laboratory in America.

A transistor is a semiconductor device, commonly used as an Amplifier or an electrically controlled switch.

There are two types of transistors:

Unipolar Junction Transistor

Bipolar Junction Transistor

In Unipolar transistor, the current conduction is only due to one type of carriers i.e., majority charge carriers. The current conduction in bipolar transistor is because of both the types of charge carriers i.e., holes and electrons. Hence it is called as Bipolar Junction Transistor and it is referred to as BJT.

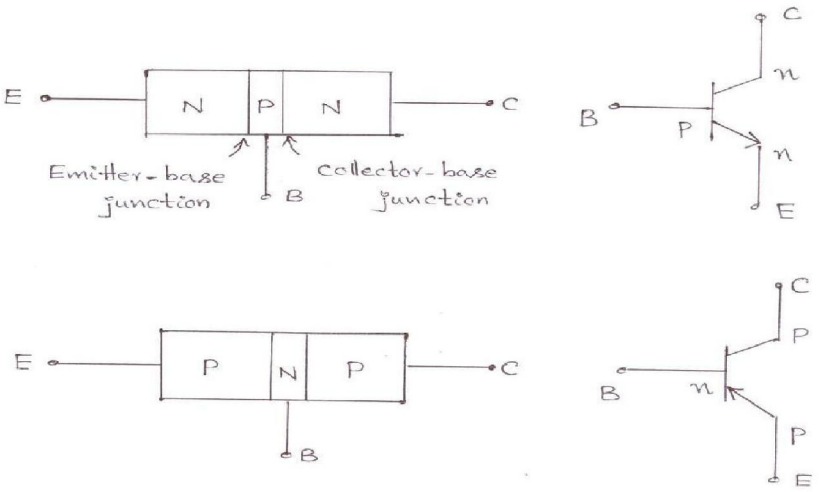
BJT is a semiconductor device in which one type of semiconductor material is sand witched between two opposite types of semiconductor i.e., an n-type semiconductor is sandwiched between two p-type semiconductors or a p-type semiconductor is sandwiched between two n-type semiconductor. Hence the BJTs are of two types.

They are:

1) n-p-n Transistor

2) p-n-p Transistor

The two types of BJTs are shown in the figure below.



The arrow head represents the conventional current direction from p to n. Transistor has three terminals.

1) Emitter

2) Base

3) Collector

Transistor has two p-n junctions. They are:

1. Emitter-Base Junction
2. Collector-Base Junction

Emitter: Emitter is heavily doped because it is to emit the charge carriers.

Base: The charge carriers emitted by the emitter should reach collector passing through the base. Hence base should be very thin and to avoid recombination, and to provide more collector current base is lightly doped.

Collector: Collector has to collect the most of charge carriers emitted by the emitter. Hence the area of cross section of collector is more compared to emitter and it is moderately doped.

Transistor can be operated in three regions.

1) Active region.

2) Saturation region.

3) Cut-Off region.

Active Region: For the transistor to operate in active region base to emitter junction is forward biased and collector to base junction is reverse biased.

Saturation Region: Transistor to be operated in saturation region if both the junctions i.e., collector to base junction and base to emitter junction are forward biased.

Cut-Off Region: For the transistor to operate in cut-off region both the junctions i.e., base to emitter junction and collector to base junction are reverse biased.

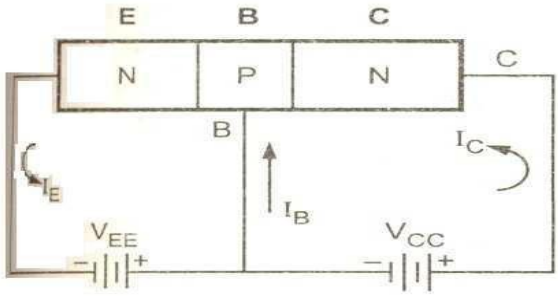
Transistor can be used as

1) Amplifier 2) Switch

For the transistor to act as an amplifier, it should be operated in active region. For the transistor to act as a switch, it should be operated in saturation region for ON state, and cut-off region for OFF state.

Transistor Operation:

Working of an n- p-n transistor:



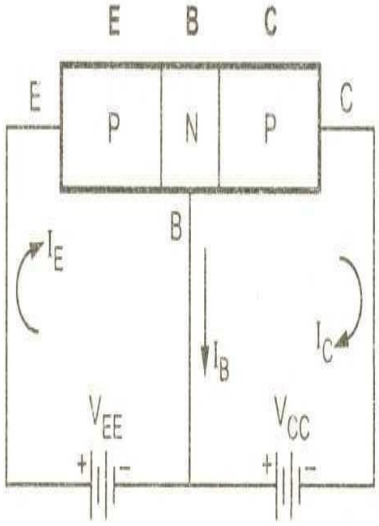
The n-p-n transistor with base to emitter junction forward biased and collector base junction reverse biased is as shown in figure.

As the base to emitter junction is forward biased the majority carriers emitted by the n-type emitter i.e., electrons have a tendency to flow towards the base which constitutes the emitter current I_E.

As the base is p-type there is chance of recombination of electrons emitted by the emitter with the holes in the p-type base. Remaining more than 95% electrons emitted by the n-type emitter cross over into the collector region constitute the collector current.

The current distributions are as shown in fig. $\mathbf{I_E = I_B + I_C}$

Working of a p-n-p transistor:



The p-n-p transistor with base to emitter junction is forward biased and collector to base junction reverse biased is as show in figure.

As the base to emitter junction is forward biased the majority carriers emitted by the p-type emitter i.e., holes have a tendency to flow towards the base which constitutes the emitter current I_E.

As the base is n-type there is a chance of recombination of holes emitted by the emitter with the electrons in the n-type base. But as the base us very thin and lightly doped only few electrons less than 5% combine with the holes emitted by the p-type emitter, the remaining 95% charge carriers cross over into the collector region to constitute the collector current.

The current distributions are shown in figure. $\mathbf{I_E = I_B + I_C}$

Current components in a transistor: The figure below shows the various current components which flow across the forward-biased emitter junction and reverse-biased collector junction in P-N-P transistor.

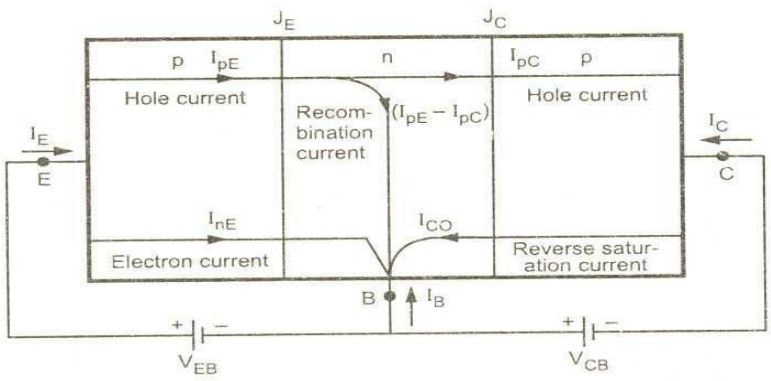


Figure: Current components in a transistor with forward-biased emitter and reverse-biased collector junctions.

The emitter current consists of the following two parts:

3. Hole current I_{pE} constituted by holes (holes crossing from emitter into base).

4. Electron current I_{nE} constituted by electrons (electrons crossing from base into the emitter).

Therefore, Total emitter current $I_E = I_{pE}$ (majority) + I_{nE} (Minority)

The holes crossing the emitter base junction J_E and reaching the collector base junction J_C

Constitutes collector current I_{pC}. Not all the holes crossing the emitter base junction J_E reach collector base junction J_C because some of them combine with the electrons in the n-type base.

Since base width is very small, most of the holes cross the collector base junction J_C and very few recombine, constituting the base current ($I_{pE} - I_{pC}$).

When the emitter is open-circuited, I_E=0, and hence I_{pC}=0. Under this condition, the base and collector together current I_C equals the reverse saturation current I_{CO}, which consists of the following two parts: I_{pCO} caused by holes moving across I_C from N-region to P-region.

I_{nCO} caused by electrons moving across I_C from P-region to N-region. $I_{CO} = I_{nCO} + I_{pCO}$

In general, $I_C = I_{nC} + I_{pC}$

Thus for a P-N-P transistor, $\mathbf{I_E = I_B + I_C}$

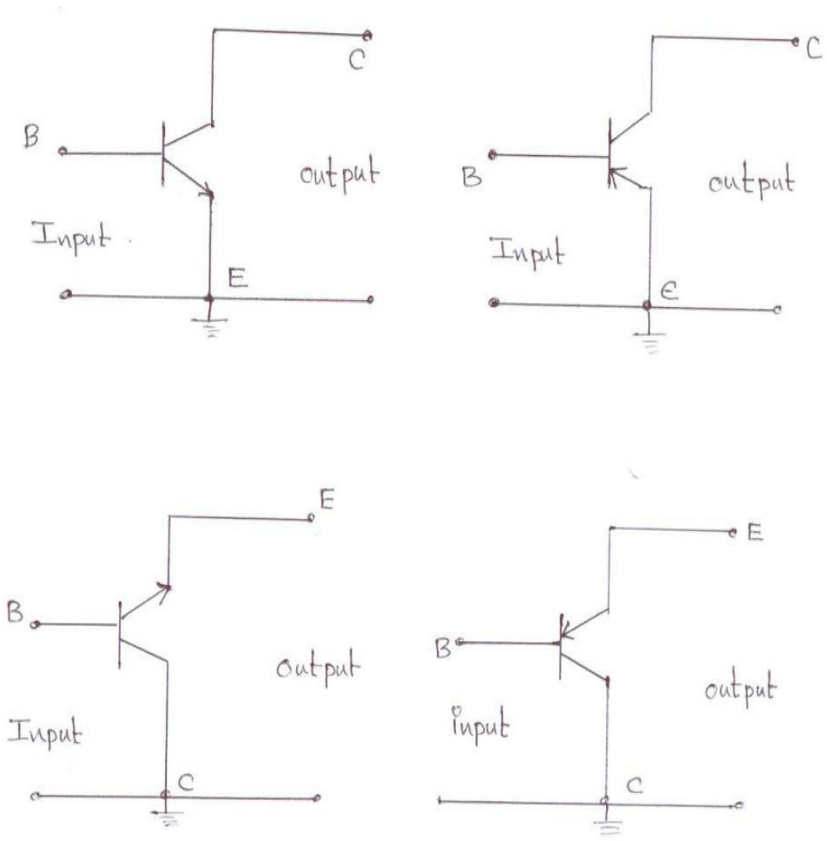
Transistor circuit configurations:

Following are the three types of transistor circuit configurations:

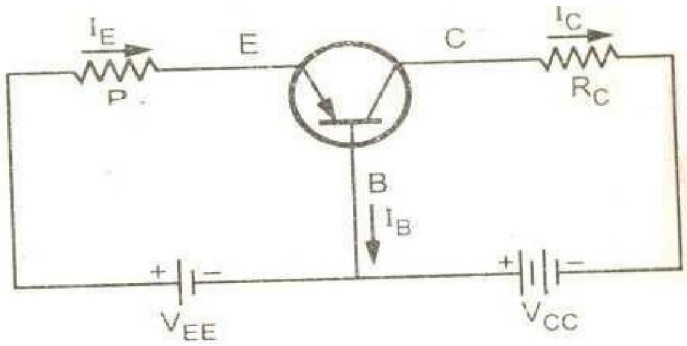
1. Common-Base (CB)
2. Common-Emitter (CE)
3. Common-Collector (CC)

Here the term 'Common' is used to denote the transistor lead which is common to the input and output circuits. The common terminal is generally grounded.

It should be remembered that regardless the circuit configuration, the emitter is always forward-biased while the collector is always reverse-biased.

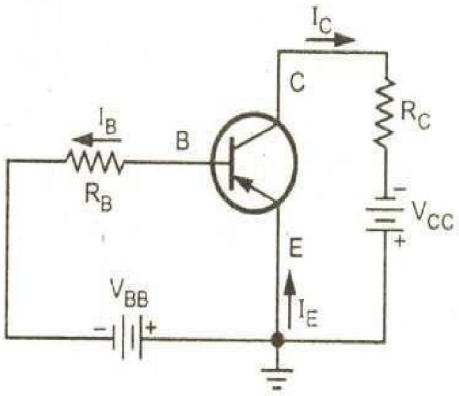


Common – Base (CB) configurations: In this configuration, the input signal is applied between emitter and base while the output is taken from collector and base. As base is common to input and output circuits, hence the name common base configuration. Figure show the common-base P-N-P transistor circuit.

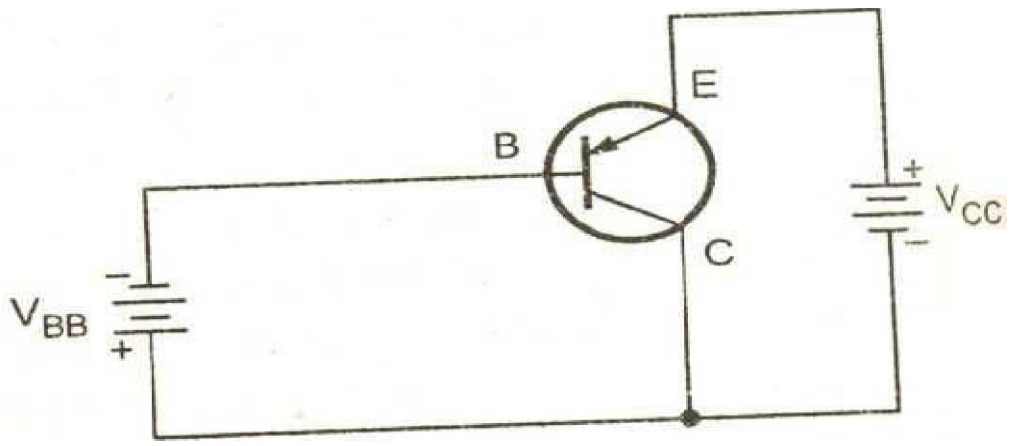


Common-Emitter (CE) configuration: In this configuration, the input signal is applied between base and emitter and the output is taken from collector and emitter. As emitter is common to input and output circuits, hence the name common emitter configuration.

Figure shows the common-emitter P-N-P transistor circuit.



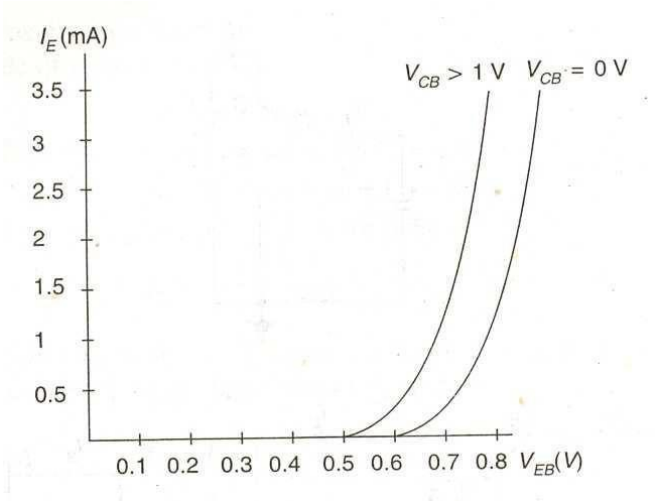
Common – Collector (CC) Configuration: In this configuration, the input signal is applied between base and collector and the output is taken from the emitter. As collector is common to input and output circuits, hence the name common collector configuration. Figure shows the common collector PNP transistor circuit.



Characteristics of Common-Base Circuit: The circuit diagram for determining the static characteristic curves of an NPN transistor in the common base configuration is shown in fig. Below

Input Characteristics: To determine the input characteristics, the collector-base voltage V_{CB} is kept constant at zero volts and the emitter current I_E is increased from zero in suitable equal steps by increasing V_{EB}. This is repeated for higher fixed values of V_{CB}. A curve is drawn between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}.

The input characteristics thus obtained are shown in figure below.



Early effect (or) Base–Width modulation:

As the collector voltage V_{CC} is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base-width on collector-to-emitter voltage is known as Early effect (or) Base-Width modulation.

Thus decrease in effective base width has following consequences:

i. Due to Early effect, the base width reduces, there is a less chance of recombination of holes with electrons in base region and hence base current I_B decreases.

ii. As I_B decreases, the collector current I_C increases.

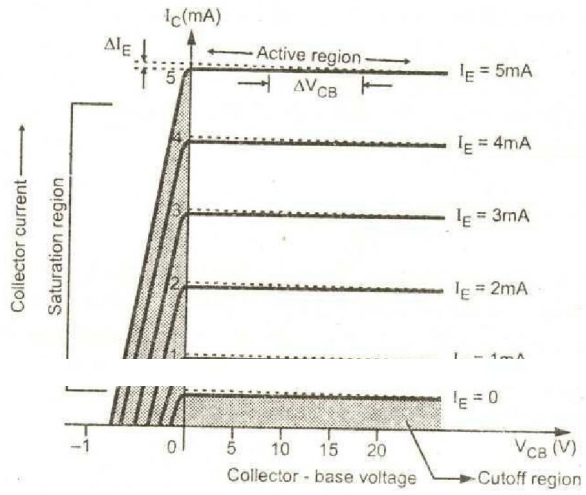
iii. As base width reduces the emitter current I_E increases for small emitter to base voltage.

iv. As collector current increases, common base current gain (□) increases.

Punch Through (or) Reach Through:

When reverse bias voltage increases more, the depletion region moves towards emitter junction and effective base width reduces to zero. This causes breakdown in the transistor. This condition is called "Punch Through" condition.

Output Characteristics: To determine the output characteristics, the emitter current I_E is kept constant at a suitable value by adjusting the emitter-base voltage V_{EB}. Then V_{CB} is increased in suitable equal steps and the collector current I_C is noted for each value of I_E. Now the curves of I_C versus V_{CB} are plotted for constant values of I_E and the output characteristics thus obtained is shown in figure below.



From the characteristics, it is seen that for a constant value of I_E, I_C is independent of V_{CB} and the curves are parallel to the axis of V_{CB}. Further, I_C flows even when V_{CB} is equal to zero. As the emitter-base junction is forward biased, the majority carriers, i.e., electrons, from the emitter are injected into the base region. Due to the action of the internal potential barrier at the reverse biased collector-base junction, they flow to the collector region and give rise to I_C even when V_{CB} is equal to zero

Transistor Parameters: The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common base hybrid parameters (or) h-parameters.

Input Impedance (h_{ib}): It is defined as the ratio of change in (input) emitter to base voltage to the change in (input) emitter current with the (output) collector to base voltage kept constant.

Output Admittance (h_{ob}): It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector-base voltage, keeping the (input) emitter current I_E constant.

Forward Current Gain (h_{fb}): It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) emitter current keeping the (output) collector voltage V_{CB} constant.

Reverse Voltage Gain (h_{rb}): It is defined as a ratio of the change in the (input) emitter voltage and the corresponding change in (output) collector voltage with constant (input) emitter current

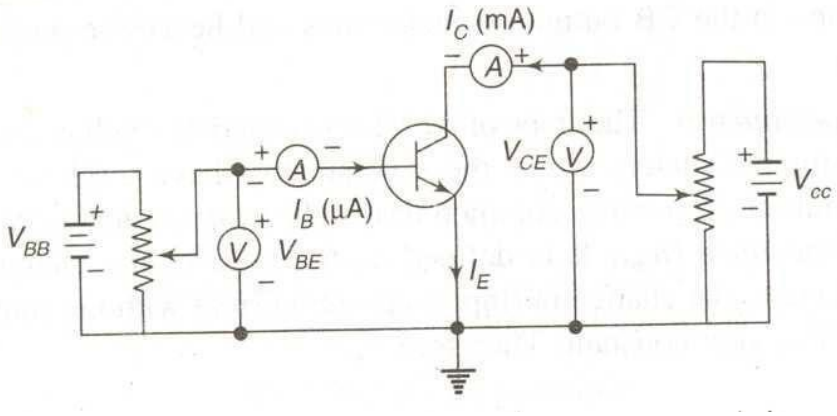
Characteristics of Common-Emitter Circuit:

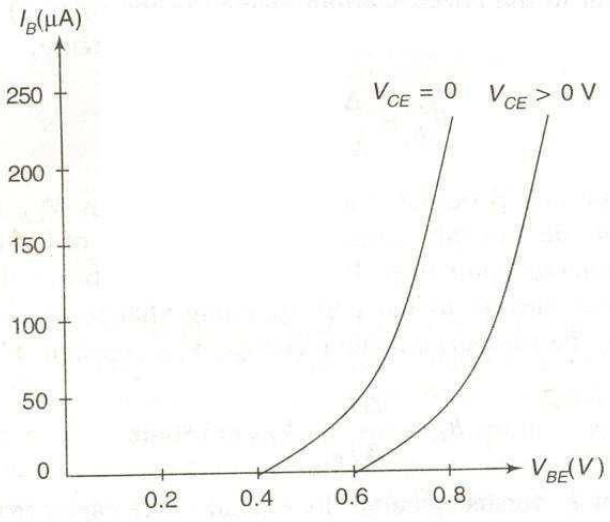
The circuit diagram for determining the static characteristic curves of the an N-P-N transistor in the common emitter configuration is shown in figure below.

Input Characteristics:

To determine the input characteristics, the collector to emitter voltage is kept constant at zero volts and base current is increased from zero in equal steps by increasing V_{BE} in the circuit. The value of V_{BE} is noted for each setting of I_B. This procedure is repeated for higher fixed values of V_{CE}, and the curves of I_B versus V_{BE} are drawn.

The input characteristics thus obtained are shown in figure below.

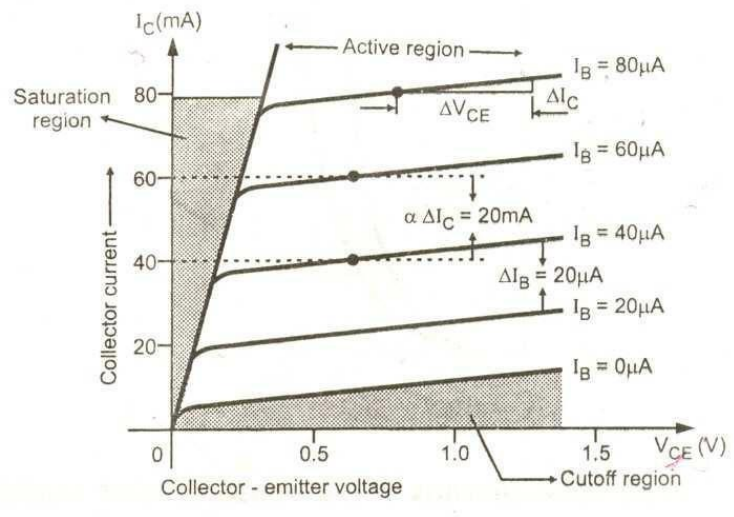




When V_{CE}=0, the emitter-base junction is forward biased and he junction behaves as a forward biased diode. When V_{CE} is increased, the width of the depletion region at the reverse biased collector-base junction will increase. Hence the effective width of the base will decrease. This effect causes a decrease in the base current I_B. Hence, to get the same value of I_B as that for V_{CE}=0, V_{BE} should be increased. Therefore, the curve shifts to the right as V_{CE} increases.

Output Characteristics:

To determine the output characteristics, the base current I_B is kept constant at a suitable value by adjusting base-emitter voltage, V_{BE}. The magnitude of collector-emitter voltage V_{CE} is increased in suitable equal steps from zero and the collector current I_C is noted for each setting of V_{CE}. Now the curves of I_C versus V_{CE} are plotted for different constant values of I_B. The output Characteristics thus obtained are shown in figure below.



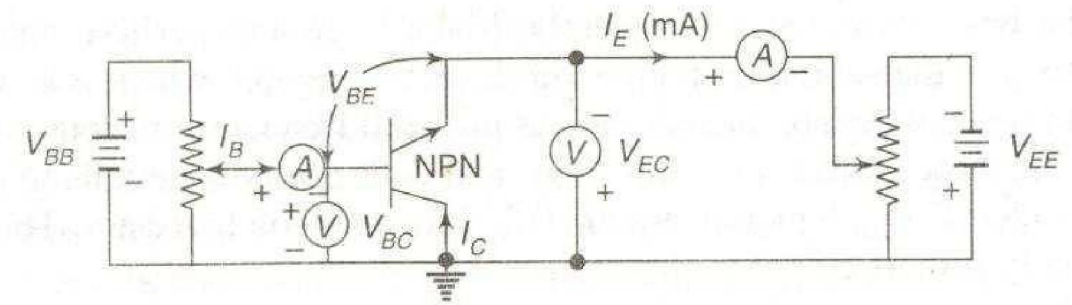
The output characteristics of common emitter configuration consist of three regions: Active, Saturation and Cut-off regions.

Active Region: The region where the curves are approximately horizontal is the "Active" region of the CE configuration. In the active region, the collector junction is reverse biased. As V_{CE} is increased, reverse bias increase. This causes depletion region to spread more in base than in collector, reducing the changes of recombination in the base. This increase the value of β_{dc} . This Early effect causes collector current to rise more sharply with increasing V_{CE} in the active region of output characteristics of CE transistor.

Saturation Region: If V_{CE} is reduced to a small value such as 0.2V, then collector-base junction becomes forward biased, since the emitter-base junction is already forward biased by 0.7V. The input junction in CE configuration is base to emitter junction, which is always forward biased to operate transistor in active region. Thus input characteristics of CE configuration are similar to forward characteristics of p-n junction diode. When both the junctions are forwards biased, the transistor operates in the saturation region, which is indicated on the output characteristics. The saturation value of V_{CE}, designated $V_{CE(Sat)}$, usually ranges between 0.1V to 0.3V.

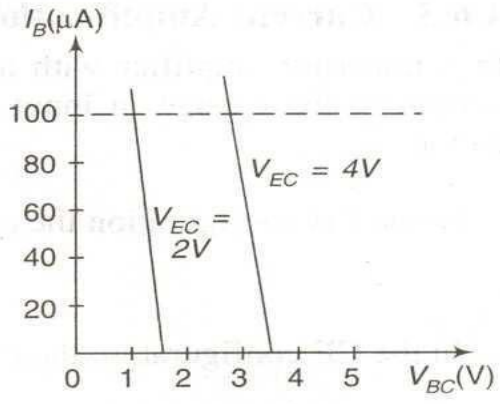
Cut-Off Region: When the input base current is made equal to zero, the collector current is the reverse leakage current I_{CEO}. Accordingly, in order to cut off the transistor, it is not enough to reduce I_B=0. Instead, it is necessary to reverse bias the emitter junction slightly. We shall define cut off as the condition where the collector current is equal to the reverse saturation current I_{CO} and the emitter current is zero.

Characteristics of common collector circuit: The circuit diagram for determining the static characteristics of an N-P-N transistor in the common collector configuration is shown in fig. below.

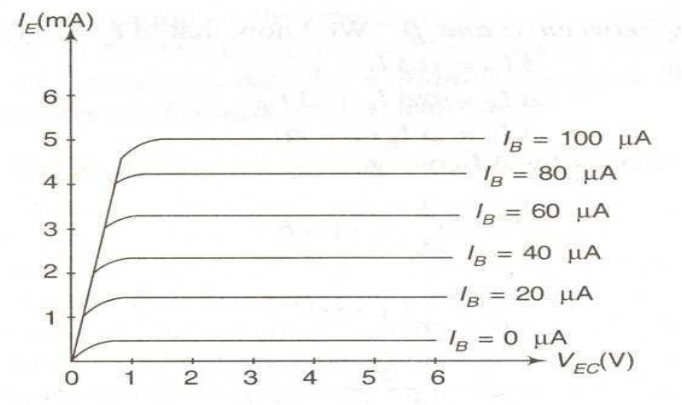


Input Characteristics:

To determine the input characteristic, V_{EC} is kept at a suitable fixed value. The base-collector voltage V_{BC} is increased in equal steps and the corresponding increase in I_B is noted. This is repeated for different fixed values of V_{EC}. Plots of V_{BC} versus I_B for different values of V_{EC} shown in figure are the input characteristics.



Output Characteristics: The output characteristics shown in figure below are the same as those of the common emitter configuration.



BIASING

Introduction:

The basic function transistor is to do amplification. The process of raising the strength of a weak signal without any change in its shape is known as faithful amplification.

For faithful amplification, the following three conditions must be satisfied:

The emitter-base junction should be forward biased,

The collector-base junction should be reverse biased.

Three should be proper zero signal collector current.

The proper flow of zero signal collector current (proper operating point of a transistor) and the maintenance of proper collector-emitter voltage during the passage of signal is known as 'transistor biasing'.

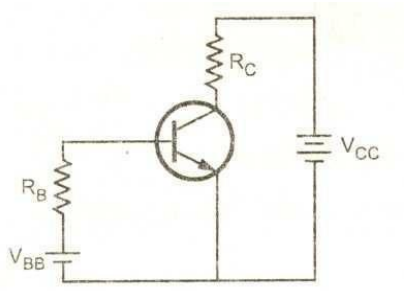
When a transistor is not properly biased, it work inefficiently and produces distortion in the output signal. Hence a transistor is to be biased correctly. A transistor is biased either with the help of battery (or) associating a circuit with the transistor. The latter method is generally employed. The circuit used with the transistor is known as biasing circuit.

In order to produce distortion-free output in amplifier circuits, the supply voltages and resistances in the circuit must be suitably chose. These voltages and resistances establish a set of d.c. voltage V_{CEQ} and current I_{CQ} to operate the transistor in the active region. These voltages and currents are called quiescent values which determine the operating point (or) Q-Point for the transistor.

The process of giving proper supply voltages and resistances for obtaining the desired Q-Point is called biasing.

DC Load Line:

Consider common emitter configuration circuit shown in figure below:



In transistor circuit analysis generally it is required to determine the value of I_C for any desired value of V_{CE}. From the load line method, we can determine the value of I_C for any desired value of V_{CE}. The output characteristic of CE configuration is shown in figure below:

Operating Point (or) Quiescent Point:

In designing a circuit, a point on the load line is selected as the dc bias point (or) quiescent point. The Q-Point specifies the collector current I_C and collector to emitter voltage V_{CE} that exists when no input signal is applied.

The dc bias point (or) quiescent point is the point on the load line which represents the current in a transistor and the voltage across it when no signal is applied. The zero signal values of I_C ad V_{CE} are known as the operating point.

Biasing:

The process of giving proper supply voltages and resistances for obtaining the desired Q-point is called 'biasing'.

Stabilization

The maintenance of operating point stable is known as '*STABILIZATION'.*

There are two factors which are responsible for shifting the operating point. They are:

1) The transistor parameters are temperature dependent.
2) When a transistor is replaced by another of same type, there is a wide spread in the values of transistor parameters.

So, stabilization of the operating point is necessary due to the following reasons:

1. Temperature dependence of I_C.
2. Individual variations and
3. Thermal runaway.

Temperature dependence of I_C:

The instability of I_C is principally caused by the following three sources:

ii) The I_{CO} doubles for every 10^oC rise in temperature.
iii) Increase of β with increase of temperature.
iv) The V_{BE} decreases about 2.5mV per ^oC increase in temperature.

Individual variations:

When a transistor is replaced by another transistor of the same type, the values of β and V_{BE} are not exactly the same. Hence the operating point is changed. So it is necessary to stabilize the operating point irrespective of individual variations in transistors parameters.

Thermal Runaway:

Depending upon the construction of a transistor, the collector junction can withstand maximum temperature. The range of temperature lies between 60^oC to 100^oC for 'Ge' transistor and 150^oC to 225^oC for 'Si' transistor. If the temperature increases beyond this range then the transistor burns out. The increase in the collector junction temperature is due to thermal runaway.

When a collector current flows in a transistor, it is heated i.e., its temperature increases. If no stabilization is done, the collector leakage current also increases. This further increases the transistor temperature. Consequently, there is a further increase in collector leakage current. The action becomes cumulative and the transistor may ultimately burn out. The self-destruction of an unstabilized transistor is known as thermal runaway.

The following two techniques are used for stabilization.

1) Stabilization techniques:

The technique consists in the use of a resistive biasing circuit which permits such a variation of base current I_B as to maintain I_C almost constant in spite of I_{CO}, β and V_{BE}.

2) Compensation techniques:

In this technique, temperature sensitive devices such as diodes, thermistors and sensistors etc., are used. Such devices produce compensating voltages and current in such a way that the operating points maintained stable

Stability factors:

Since there are three variables which are temperature dependent, we can define three stability factors as below:

i) **S:** The stability factor 'S' is defined as the ration of change of collector current I_C with the reverse saturation current IC_0, keeping β and V_{BE} constant.

ii) **S' :** The stability factor S' is defined as the rate of change of I_C with respect to V_{BE}, keeping I_{CO} and β constant

iii) ***S'' :*** *The stability factor S'' is defined as the rate of change of I_C with respect to β, keeping I_{CO} and V_{BE} constant.*

Fixed bias (or) base resistor method:

A CE amplifier used fixed bias circuit is shown in figure below:

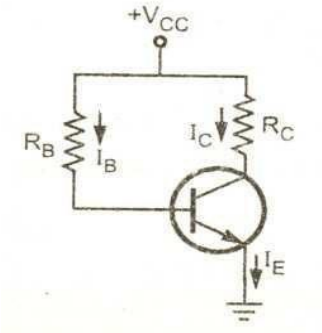


Fig: Fixed bias circuit.

In this method, a high resistance R_B is connected between positive terminal of supply V_{CC} and base of the transistor. Here the required zero signal base current flows through R_B and is provided by V_{CC}.

In figure, the base-emitter junction is forward biased because the base is positive w.r.t. emitter. By a proper selection of R_B, the required zero signal base current (and hence $I_C=\beta I_B$) can be made to flow.

Advantages of fixed bias circuit:

1. This is a simple circuit which uses very few components.
2. The operating point can be fixed anywhere in the active region of the characteristics by simply changing the values of R_B. Thus, it provides maximum flexibility in the design.

Disadvantages of fixed bias circuit:

1. With the rise in temperature the operating point if not stable.
2. When the transistor is replaced by another with different value of β, the operating point with shift i.e., the stabilization of operating point is very poor in fixed bias circuit.

Because of these disadvantages, fixed bias circuit required some modifications. In the modified circuit, R_B is connected between collector and base. Hence the circuit is called 'collector to base' bias circuit.

Collector to Base bias (or) Biasing with feedback resistor:

A CE amplifier using collector to base bias circuit is shown in the figure. In this method, the biasing resistor is connected between the collector and the base of the transistor.

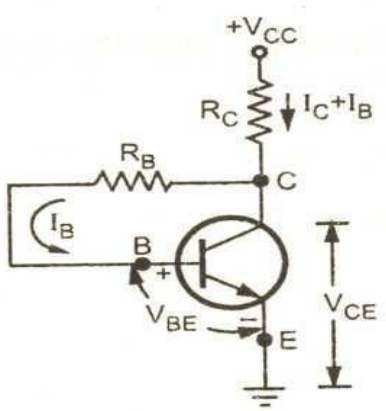


Fig: Collector–to–Base bias circuit.

Voltage Divider Bias (Or) Self-Bias (Or) Emitter Bias:

The voltage divider bias circuit is shown in figure.

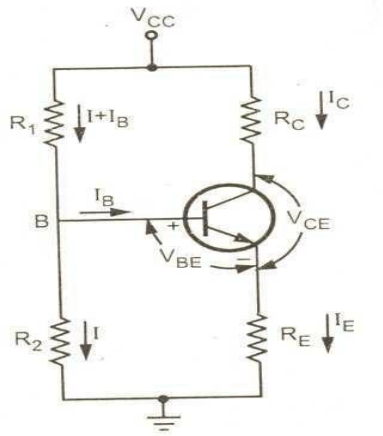


Fig: Voltage divider bias circuit.

In this method, the biasing is provided by three resistors R_1, R_2 and R_E. The resistors R_1 and R_2 acts as a potential divider giving a fixed voltage to the base.

If collector current increases due to change in temperature (or) change in β, the emitter current I_E also increases and the voltage drop across R_E increases, reducing the voltage difference between base and emitter (V_{BE}).

Due to reduction in V_{BE}, base current I_B and hence collector current I_C is also reduces. Therefore, we can say that negative feedback exists in the emitter bias circuit. This reduction in collector current I_C components for the original change in I_C

FILED EFFECT TRANSISTOR:

The filed effect transistor (abbreviated as FET) is a three terminal uni-polar semiconductor device in which current is controlled by an electric field. As current conduction is only by majority carriers, FET is said to be a uni-polar device.

Based on the construction, the FET can be classified into two types as:

x) Junction Field Effect Transistor (JFET)
xi) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) or Insulated Gate Field Effect Transistor (IGFET)

Depending upon the majority carriers, JFET has been classified into two types, namely,

iii) N-Channel JFET with electrons as the majority carriers, and
iv) P-Channel JFET with holes as the majority carriers.

Construction of N-Channel JFET:

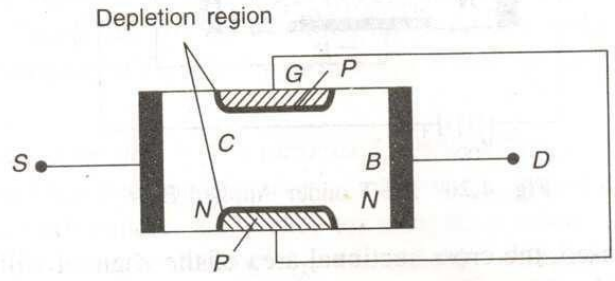
It consists of a N-type bar which is made of Silicon. Ohmic contacts (terminals), made at the two ends of the bar, are called Source and Drain.

Source (S) : This terminal is connected to the negative pole of the battery. Electronics which are the majority carriers in the N-type bar enter the bar through this terminal.

Drain (D) : This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal.

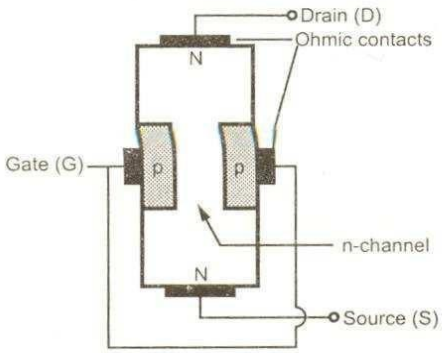
Gate (G) : Heavily doped P-type silicon is diffused on both sides of the N-type silicon bar by which PN junctions are formed. These layers are joined together are called Gate(G).

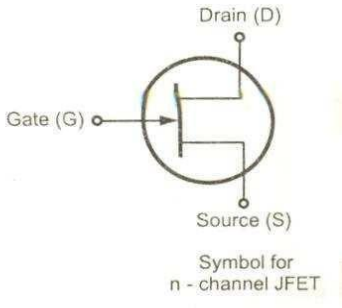
Channel : The region BC of the N-type bar between the depletion regions is called the Channel. Majority carriers move from the source to drain when a potential difference V_{DS} is applied between the source and drain



Structure and symbol of n-channel JFET:

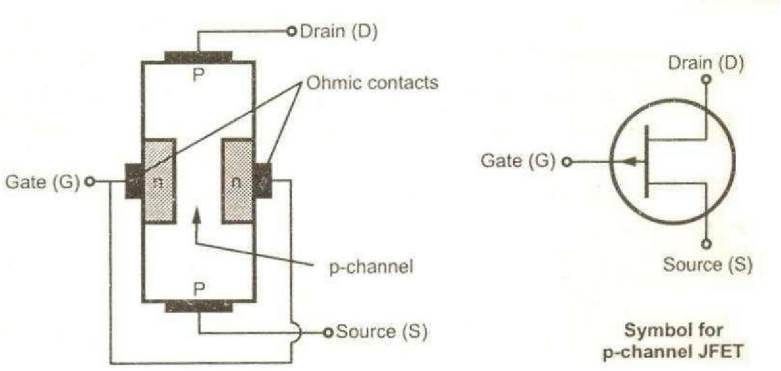
The structure and symbol of n-channel JFET are shown in figure below.





The electrons enter the channel through the terminal called 'source' and leave through the terminal called 'drain'. The terminals taken out from heavily doped electrodes of p-type material are called 'gates'. Usually, these electrodes are connected together and only one terminal is taken out, which is called 'gate

Structure and Symbol of P-Channel JFET:



The structure and symbol of P-Channel JFET is shown in the figure. The device could be made of P- type bar with two N-type gates as shown in the figure. Then this will be P-Channel JFET is similar; the only difference being that in N-Channel JFET the current is carried by the electrons while in P- Channel JFET, it is carried by holes

Operation of N-Channel JFET:

The operation of N-Channel JFET can be understood with the help of figure below.

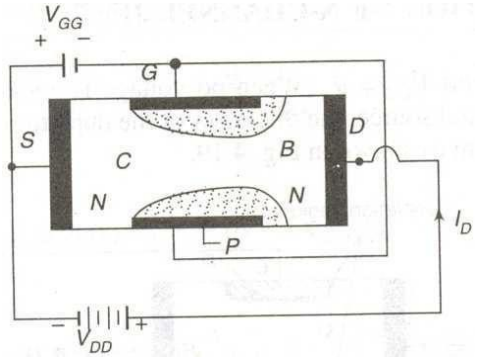
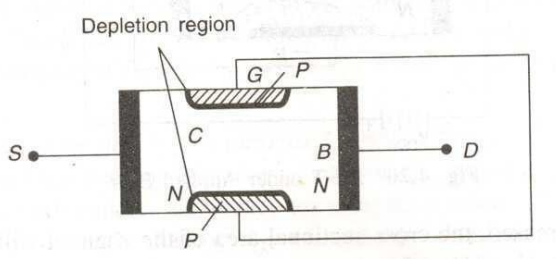


Fig. Operation of FET.

Before considering the operation, let us consider that how the depletion layers are formed. Let us first suppose that the gate has been reverse-biased by gate battery V_{GG} and the drain battery V_{DD} is not connected.

When V_{GS}=0 and V_{DS}=0:

When no voltage is applied between drain and source, and gate and source, the thickness of the depletion regions round the P-N junction is uniform as shown in figure below.



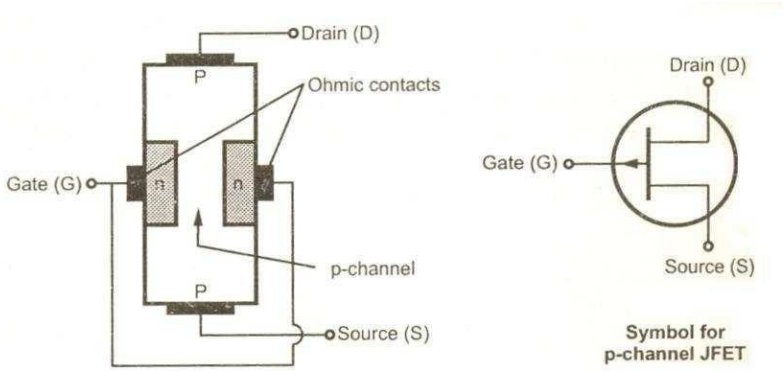
When V_{DS}=0 and V_{GS} is decreased from zero:

In this case, the P-N junctions are reverse-biased and hence the thickness of the depletion region increases. As V_{GS} is decreased from zero, the reverse bias voltage across the P-N junction is increased and hence, the thickness of the depletion region in the channel increases until the two depletion regions make contact with each other. In this condition, the channel is said to be cut-off. The value of V_{GS} which is required to cut-off the channel is called the cut-off voltage V_C.

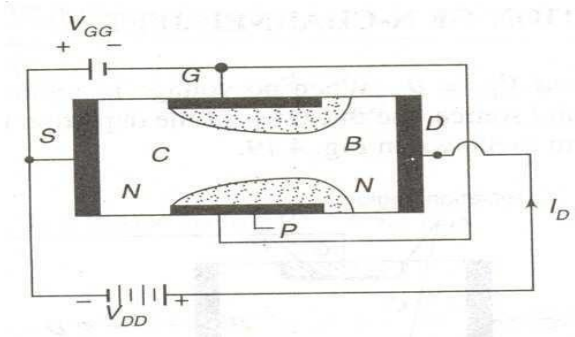
When V_{GS}=0 and V_{DS} is increased from zero:

Drain is positive with respect to the source. Now the majority carriers (electrons) flow through the N-Channel from source to drain. Therefore the conventional current I_D flows from drain to source. The magnitude of the current will depend upon the following factors:

1. The conductivity of the channel.
2. The length of the channel.
3. The cross sectional area 'A' of the channel.
4. The magnitude of the applied voltage V_{DS}.



Where 'ρ' is the resistivity of the channel. As V_{DS} increases, the reverse voltage across the P-N junction increase and hence the thickness of the depletion region also increases. Therefore, the channel is wedge shaped as shown in fig. below.



As V_{DS} is increase, at a certain value V_P of V_{DS}, the cross sectional area of the channel becomes minimum. At this voltage, the channel is said to be pinched off and the drain voltage V_P is called the pinch-off voltage.

As a result of the decreasing cross-section of the channel with the increase of V_{DS}, the following results are obtained.

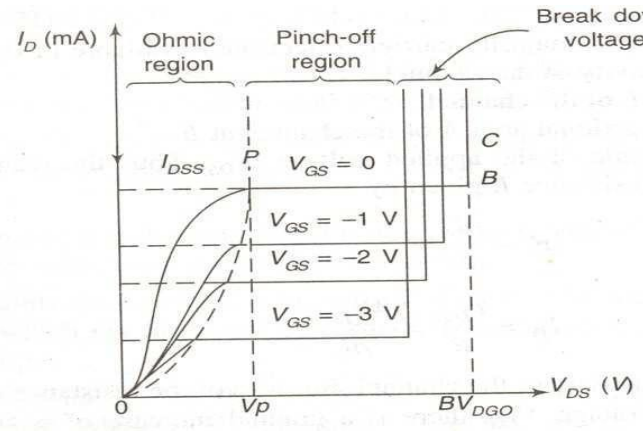


Fig. Drain characteristics

i) As V_{DS} is increased from zero, I_D increases linearly along OP, this region from V_{DS}=0 to V_{DS}=V_P is called the ohmic region. In this region, the FET acts as a voltage variable resistor (VVR) or voltage dependent resistor (VDR).

ii) When V_{DS}=V_P, I_D becomes maximum. When V_{DS} is increased beyond V_P, the length of the pinch-off (or) saturation region increases. Hence, there is no further increase of I_D.

iii) At a certain voltage corresponding to the point B, I_D suddenly increases. This effect is due to the Avalanche multiplication of electrons caused by breaking of covalent bonds of silicon atoms in the depletion region between the gate and the drain. The drain voltage at which the breakdown occurs is denoted by B_{vdo}.

When V_{GS} is negative and V_{DS} is increased:

When the gate is maintained at a negative voltage less than the negative cut-off voltage, the reverse voltage across the junction is further increased. Hence for a negative value of V_{GS}, the curve of I_D versus V_{DS} is similar to that for V_{GS}=0, but the values of V_P and BV_{DGO} are lower.

The drain current I_D is controlled by the electric field that extends into the channel due to reverse biased voltage applied to the gate, hence, this device has been given the name Field Effect Transistor.

Comparison of JEFT and BJT

i) FET operation depends only on the flow of majority carriers – holes for p-channel FET's and electrons for N-channel FET's. Therefore, they are called Uni-Polar devices. Bipolar transistor (BJT) operation depends on both minority and majority current devices.

ii) As FET has no junctions and the conduction is through an N-type (or) P-type semiconductor material, FET is less noisy than BJT.

iii) As the input circuit of FET is reverse biased, FET exhibits a much higher input impedance (in the order of 100MΩ) and lower output impedance and there will be a high degree of isolation between input and output. So, FET can acts as an excellent buffer amplifier but the BJT has low input impedance because its input circuit is forwards biased.

iv) FET is a voltage controlled device, i.e., voltage at the input terminal controls the output current, whereas BJT is a current controlled device, i.e., the input current controls the output current.

v) FET's are much easier to fabricate and are particularly suitable for IC's because they occupy less space than BJT's.

vi) The performance of BJT is degraded by neutron radiation because of the reduction in minority-carrier life time, whereas FET can tolerate a much higher level of radiation since they do not rely on minority carriers for their operation.

vii) The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature co-efficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature co-efficient at high current levels which leads to thermal breakdown

viii) Since FET does not suffer from minority carrier storage effects, it has higher switching speeds and cut-off frequencies. BJT suffers from minority carrier storage effects and therefore has lower switching speed and cut-off frequencies.

ix) FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.

x) BJT's are cheaper to produce than FET's.

Applications of JFET

1. FET is used as a buffer in measuring instruments, receivers since it has high input impedance and low output impedance.

2. FET's are used in Radio Frequency amplifiers in FM (Frequency Mode) tuners and communication equipment for the low noise level.

3. Since the input capacitance is low, FET's are used in cascade amplifiers in measuring and test equipments.

4. Since the device is voltage controlled, it is used as voltage variable resistor in operational amplifiers and tone controls

5. FET's are used in mixer circuits in FM and TV receivers, and communication equipments because inter modulation distortion is low.
6. It is used in oscillator circuits because frequency drift is low.

7. As the coupling capacitor is small, FET's are used in low frequency amplifiers in hearing aids and inductive transducers.
8. FET's are used in digital circuits in computers, LSD and a memory circuit because of it is small size.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

MOSFET is the common term for the Insulated Gate Field Effect Transistor (IGFET). There are two basic forms of MOSFET, they are:

i) Enhancement MOSFET and
ii) Depletion MOSFET

Principle:

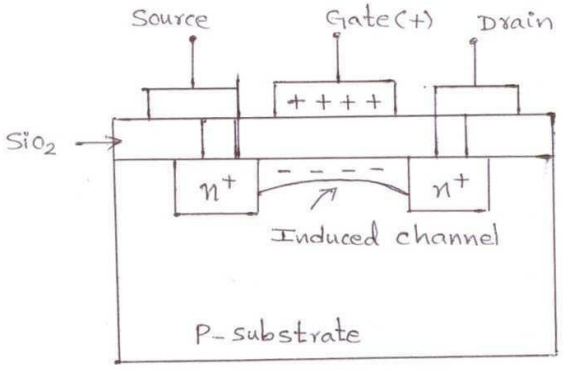
By applying a transverse electric field across an insulator, deposited on the semi conducting material, the thickness and hence the resistance of conducting channel of a semi conducting material can be controlled.

In depletion MOSFET, the controlling electric field reduces the number of majority carriers available for conduction, whereas in the enhancement MOSFET, application of electric field causes an increase in the majority carrier density in the conducting regions of the transistor.

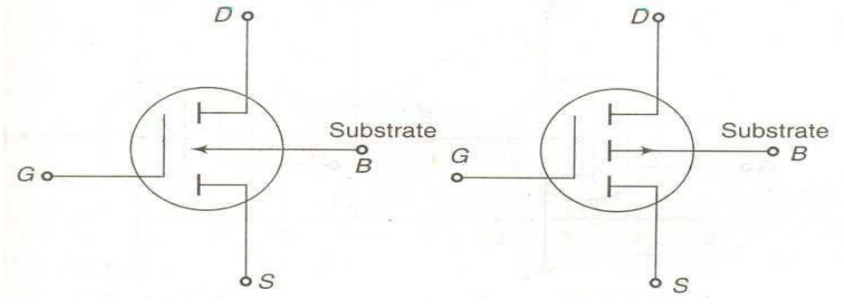
Enhancement MOSFET

Construction:

The construction of an N-channel enhancement MOSFET is shown in figure (a) below and the circuit symbols for an N-Channel and a P-channel enhancement MOSFET are shown in figures (b) and (c) respectively. As there is no continuous channel in an enhancement MOSFET



(a)



(b) N-Channel (c) P-Channel

Fig. (a) N-Channel Enhancement MOSFET
(b) and (c) Circuit symbols for enhancement MOSFET

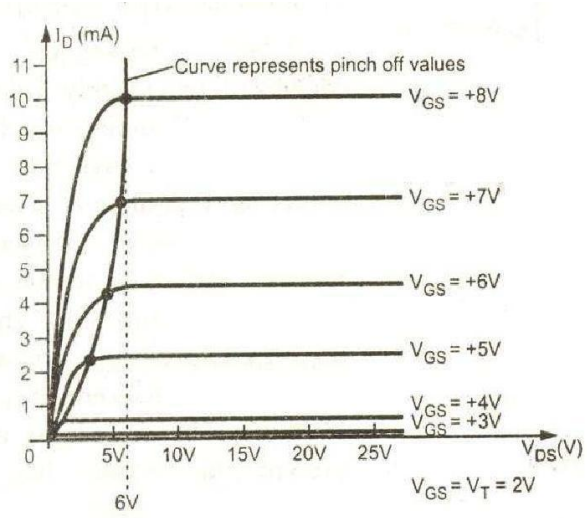
Two highly doped N^+ regions are diffused in a lightly doped substrate of p-type silicon. One N^+ region is called the source S and the other one is called the drain D. They are separated by 1 milli (10^{-3} inch). A thin insulating layer of SiO_2 is grown over the surface of the structure and holes are cut into the oxide layer, allowing contact with source and drain. Then a thin layer of metal aluminum is formed over the layer of SiO_2. Thus metal layer covers the entire channel region and it forms the gate G.

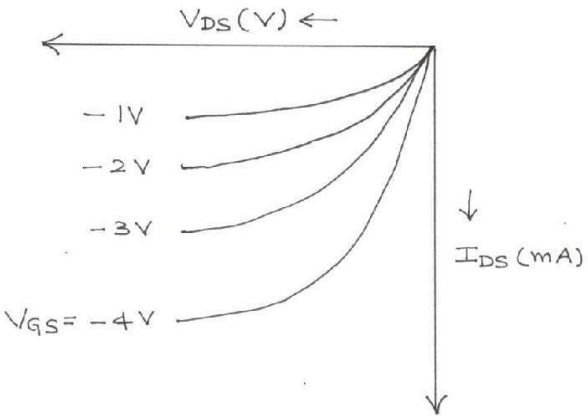
The metal area of the gate, in conjunction with the insulating oxide layer of SiO_2 and the semi conductor channel forms a parallel plate capacitor. This device is called the insulated gate FET because of the insulating layer of SiO_2. This layer gives extremely high input impedance for the MOSFET.

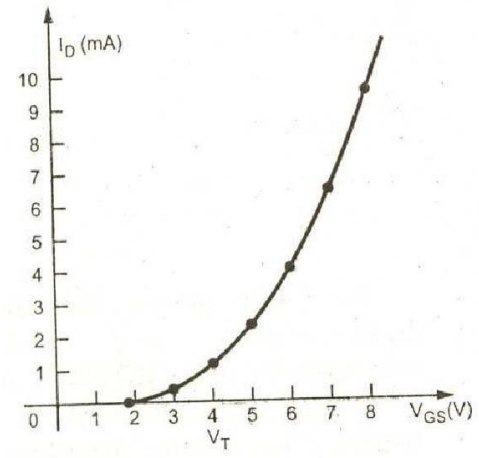
Operation:

If the substrate is grounded and a positive voltage is applied at the gate, the positive charge on G induces an equal negative charge on the substrate side between the sourced drain regions. Thus, an electric field is produced between the source and drain regions. The direction of the electric field is perpendicular to the plates of the capacitor through the oxide. .

The negative charge of electrons which are minority carriers in the p-type substrate forms an inversion layer. As the positive voltage on the gate increases, the induced negative charge in the semi conductor increases. Hence, the conductivity increases and current flows from source to drain through the induced channel. Thus the drain current is enhanced by the positive gate







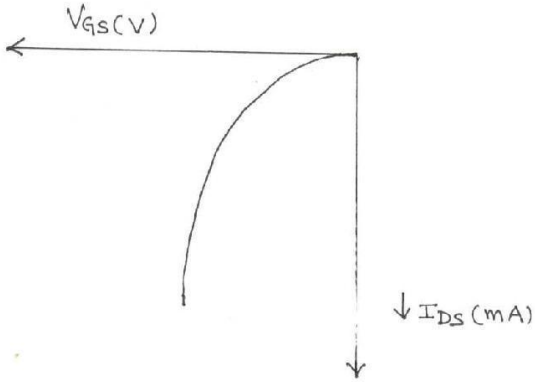


Fig: V-I (or) drain characteristics of MOSFET.

(a) n-channel enhancement MOSFET
(b) p-channel enhancement MOSFET

Fig: Transfer characteristics of MOSFET.

(a) n-channel enhancement MOSFET

(b) p-channel enhancement MOSFET

Depletion MOSFET:

Construction:

The construction of an N-channel where an N-channel is diffused between the source and drain to the basic structure of MOSFET. The circuit symbols for an N-channel and P-channel depletion MOSFET are shown in figure (b) and (c) respectively.

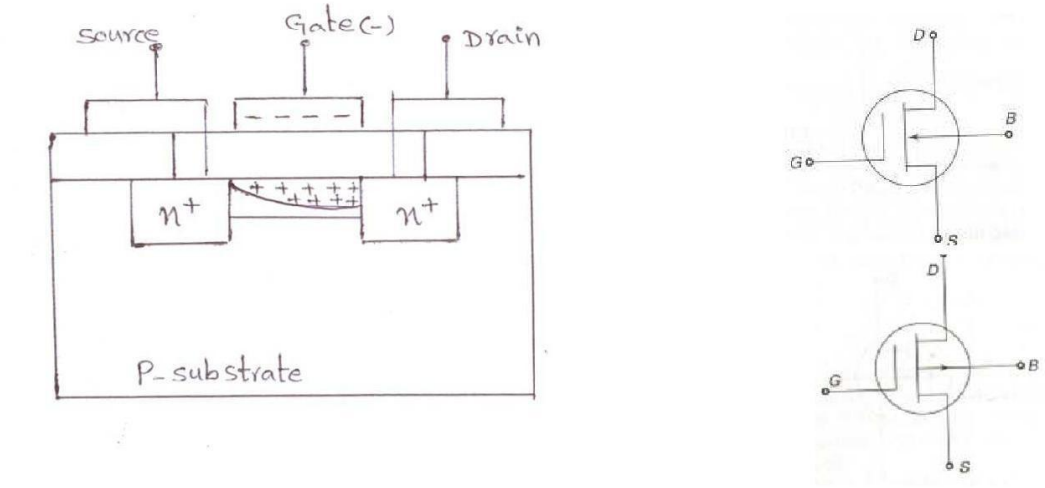


Fig (a) N-channel depletion MOSFET (b) N -channel & P-channel circuit symbols.

When V_{GS}=0 and the drain D at a positive potential with respect to the source, the electrons (majority carriers) flow through the n-channel from source to drain. Therefore, the

Conventional current I_D flows through the channel from drain to source.

If gate voltage is made negative, positive charge consisting of holes is induced in the channel through SiO_2 of the gate-channel capacitor. The introduction of the positive charge causes

depletion of mobile electrons in the channel. Thus a depletion region is produced in the channel.

The shape of the depletion region depends on V_{GS} and V_{DS}. Hence the channel will be wedge shaped as shown in figure.

When V_{DS} is increased, I_D increases and it becomes practically constant at a certain value of V_{DS}, called the pinch-off voltage. The drain current I_D almost gets saturated beyond the pinch- off voltage.

The depletion MOSFET may also be operated in an enhancement mode: It is only necessary to apply a positive gate voltage so that negative charges are induced into the n-type channel.

Hence, the conductivity of the channel increases and I_D increases. As the depletion MOSFET can be operated with bipolar input signals irrespective of doping of the channel, it is also called as dual

mode MOSFET.

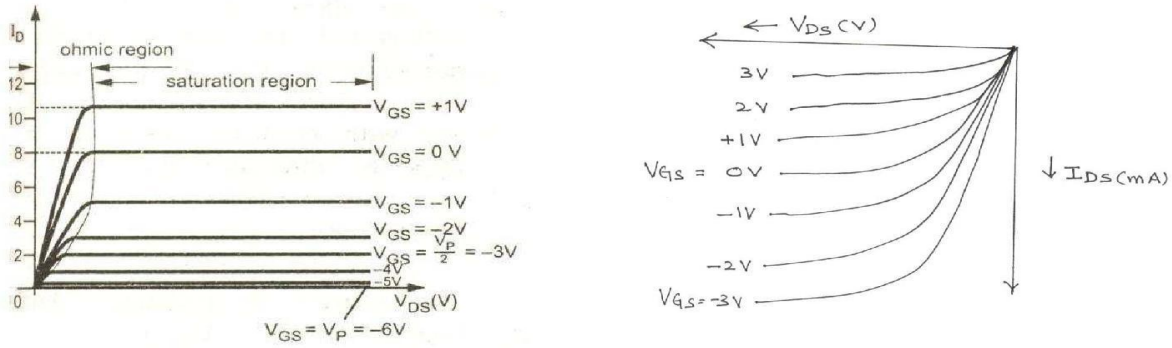


Fig: Drain characteristics of MOSFET.

(a) n-channel depletion MOSFET (b) p -channel depletion MOSFET

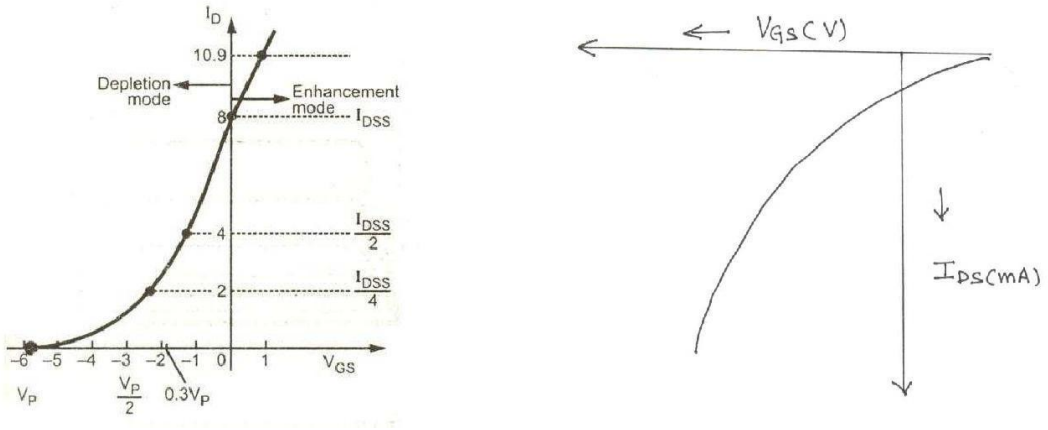


Fig: Transfer characteristics of MOSFET.

(a) n-channel depletion MOSFET
(b) p-channel depletion MOSFET

Comparison of MOSFET with JFET

i) In enhancement and depletion types of MOSFET, the transverse electric field induced across an insulating layer deposited on the semi conductor material controls the conductivity of the channel. In the JFET the transverse electric field across the reverse biased PN-junction controls the conductivity of the channel.

ii) The gate leakage current in a MOSFET is of the order of 10^{-12} A. Hence the input resistance of a MOSFET is very high in the order of 10^{10} to 10^{15} Ω. The gate leakage current of a JFET is of the order of 10^{-9} A and its input resistance is of the order of 10^{8} Ω.

iii) The output characteristics of the JFET are flatter than those of the MOSFET and hence, the drain resistance of a JFET (0.1 to 1MΩ) is much higher than that of a MOSFET (1 to 50KΩ).

iv) JFET's are operated only in the depletion mode. The depletion type MOSFET may be operated in both depletion and enhancement mode.

v) Comparing to JFET, MOSFET's are easier to fabricate.

vi) MOSFET is very susceptible to over load voltage and needs special handling during installation. It gets damaged easily if it is not properly handled.

vii) MOSFET has zero off set voltage. As it is a symmetrical device, the source and drain can be interchanged. These two properties are very useful in analog signal switching.

viii) Special digital CMOS circuits are available which involve near-zero power dissipation and very low voltage and current requirements. This makes them most suitable for portable systems.

MOSFET's are widely used in digital VLSI circuits than JFET's because of their advantage.