

**G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) KURNOOL**

**IIB.Tech II-SEM OBJECTIVE II-MID EXAM CSE**

**Sub: CO  
10 -05- 17**

**Date:**

**Time: 20 minutes  
Max.Marks:10**

**Roll NO:  
Invigilator:**

**Signature of**

**Answer all the bits, each bit carries ½ mark.**

1. Cache memory works on the principle of \_\_\_\_\_. [ ]  
a).Locality of data b)Locality of memory c) Locality of reference d) none
2. Write Through technique is used in which memory for updating the data \_\_\_\_\_. [ ]  
a)Virtual memory b)Main memory c)Auxiliary memory d)Cache memory
3. What characteristic of RAM memory makes it not suitable for permanent storage? [ ]  
a) too slow b)unreliable c) it is volatile d)too bulky
4. Which memory device is generally made of semi-conductors? [ ]  
a) RAM b) Hard-disk c) Floppy disk d) Cd disk
5. \_\_\_\_\_ is generally used to increase the apparent size of physical memory. [ ]  
a) Secondary memory b) Virtual memory c) Hard-disk d) Disks
6. When the processor receives the request from a device, it responds by sending \_\_\_\_\_. [ ]  
a) Acknowledge signal b) BUS grant signal c) Response signal d) None of the above
7. The DMA technique where the controller is given complete access to main memory is... [ ]  
a) Cycle stealing b) Memory stealing c) Memory mode d) Burst mode
8. The DMA controller has \_\_\_\_\_ registers [ ]  
A) 4 B) 2 C) 3 D) 1
9. The algorithm which replaces the block which has not been referenced for awhile is called [ ]  
A) LRU B) ORF C) Direct D) Both a and b
- 10.The number successful accesses to memory stated as a fraction is called as \_\_\_\_\_. [ ]  
A) Hit rate B) Miss rate C) Success rate D) Access rate

**G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) KURNOOL**

**IIB.Tech II-SEM OBJECTIVE II-MID EXAM CSE**

**Sub: CO  
10 -05- 17**

**Date:**

**Time: 20 minutes  
Max.Marks:10**

**Roll NO:  
Invigilator:**

**Signature of**

**Answer all the bits, each bit carries ½ mark.**

1. Cache memory works on the principle of \_\_\_\_\_. [ ]

- a).Locality of data b)Locality of memory c) Locality of reference d) none
2. Write Through technique is used in which memory for updating the data \_\_\_\_\_. [ ]  
 a)Virtual memory b)Main memory c)Auxiliary memory d)Cache memory
3. What characteristic of RAM memory makes it not suitable for permanent storage? [ ]  
 a) too slow b)unreliable c) it is volatile d)too bulky
4. Which memory device is generally made of semi-conductors? [ ]  
 a) RAM b) Hard-disk c) Floppy disk d) Cd disk
5. \_\_\_\_\_ is generally used to increase the apparent size of physical memory. [ ]  
 a) Secondary memory b) Virtual memory c) Hard-disk d) Disks
6. When the processor receives the request from a device, it responds by sending \_\_\_\_\_. [ ]  
 a) Acknowledge signal b) BUS grant signal c) Response signal d) None of the above
7. The DMA technique where the controller is given complete access to main memory is.... [ ]  
 a) Cycle stealing b) Memory stealing c) Memory mode d) Burst mode
8. The DMA controller has \_\_\_\_\_ registers [ ]  
 A) 4 B) 2 C) 3 D) 1
9. The algorithm which replaces the block which has not been referenced for awhile is called [ ]  
 A) LRU B) ORF C) Direct D) Both a and b
10. The number successful accesses to memory stated as a fraction is called as \_\_\_\_\_. [ ]  
 A) Hit rate B) Miss rate C) Success rate D) Access rate

- 11) . Resource Conflicts can be avoided by using \_\_\_\_\_ [ ]  
 A) Single memory space B) Multiple Processors C) Separate instruction & data memories D) All
12. Generally processor is the bus master \_\_\_\_\_ (TRUE/FALSE)
13. In pipelining the instructions are executed in parallel \_\_\_\_\_ (TRUE/FALSE)
14. In synchronous bus one data transfer in one bus cycle \_\_\_\_\_ (TRUE/FALSE)
15. In synchronous bus data transfer controlled by handshake signals (TRUE/FALSE)
16. Data hazard is overcome by using \_\_\_\_\_
17. PCI stands for \_\_\_\_\_
18. UMA means \_\_\_\_\_
19. Define STATIC RAM \_\_\_\_\_
20. Define pipelining \_\_\_\_\_

- 11) . Resource Conflicts can be avoided by using \_\_\_\_\_ [ ]  
 A) Single memory space B) Multiple Processors C) Separate instruction & data memories D) All
12. Generally processor is the bus master \_\_\_\_\_ (TRUE/FALSE)

13. In pipelining the instructions are executed in parallel (TRUE/FALSE)
14. In synchronous bus one data transfer in one bus cycle (TRUE/FALSE)
15. In synchronous bus data transfer controlled by handshake signals (TRUE/FALSE)
16. Data hazard is overcome by using \_\_\_\_\_
17. PCI stands for \_\_\_\_\_
18. UMA means \_\_\_\_\_
19. Define STATIC RAM \_\_\_\_\_
20. Define pipelining \_\_\_\_\_



**G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) KURNOOL**

**IIB.Tech II-SEM OBJECTIVE II-MID EXAM CSE**

**Sub: CO  
10 -05- 17**

**Date:**

**Time: 20 minutes  
Max.Marks:10**

**Roll NO:  
Invigilator:**

**Signature of**

**Answer all the bits, each bit carries ½ mark.**

1. What characteristic of RAM memory makes it not suitable for permanent storage? [ ]  
a) too slow      b)unreliable    c) it is volatile                      d)too bulky
2. Which memory device is generally made of semi-conductors? [ ]  
a) RAM b) Hard-disk c) Floppy disk d) Cd disk
3. Cache memory works on the principle of \_\_\_\_\_. [ ]  
a).Locality of data    b)Locality of memory    c) Locality of reference    d) none
4. Write Through technique is used in which memory for updating the data \_\_\_\_\_. [ ]  
a)Virtual memory b)Main memory c)Auxiliary memory                      d)Cache memory
5. \_\_\_\_\_ is generally used to increase the apparent size of physical memory. [ ]  
a) Secondary memory b) Virtual memory    c) Hard-disk    d) Disks
6. When the processor receives the request from a device, it responds by sending \_\_\_\_\_. [ ]  
a) Acknowledge signal    b) BUS grant signal    c) Response signal    d) None of the above
7. The DMA technique where the controller is given complete access to main memory is... [ ]  
a) Cycle stealing    b) Memory stealing    c) Memory mode    d) Burst mode
8. The DMA controller has \_\_\_\_\_ registers [ ]  
A) 4    B) 2    C) 3    D) 1
9. The number successful accesses to memory stated as a fraction is called as \_\_\_\_\_. [ ]  
A) Hit rate    B) Miss rate    C) Success rate    D) Access rate
10. The algorithm which replaces the block which has not been referenced for awhile is called [ ]

- A) LRU B) ORF C) Direct D) Both a and b



**G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) KURNOOL**

**IIB.Tech II-SEM OBJECTIVE II-MID EXAM CSE**

**Sub: CO  
10 -05- 17**

**Date:**

**Time: 20 minutes  
Max.Marks:10**

**Roll NO:  
Invigilator:**

**Signature of**

---

**Answer all the bits, each bit carries ½ mark.**

1. What characteristic of RAM memory makes it not suitable for permanent storage? [ ]  
a) too slow b)unreliable c) it is volatile d)too bulky
2. Which memory device is generally made of semi-conductors? [ ]  
a) RAM b) Hard-disk c) Floppy disk d) Cd disk
3. Cache memory works on the principle of \_\_\_\_\_. [ ]  
a).Locality of data b)Locality of memory c) Locality of reference d) none
4. Write Through technique is used in which memory for updating the data \_\_\_\_\_. [ ]  
a)Virtual memoryb)Main memory c)Auxiliary memory d)Cache memory
5. \_\_\_\_\_ is generally used to increase the apparent size of physical memory. [ ]  
a) Secondary memory b) Virtual memory c) Hard-disk d) Disks
6. When the processor receives the request from a device, it responds by sending \_\_\_\_\_. [ ]  
a) Acknowledge signal b) BUS grant signal c) Response signal d) None of the above
7. The DMA technique where the controller is given complete access to main memory is.... [ ]  
a) Cycle stealing b) Memory stealing c) Memory mode d) Burst mode
8. The DMA controller has \_\_\_\_\_ registers [ ]  
A) 4 B) 2 C) 3 D) 1
- 9.The number successful accesses to memory stated as a fraction is called as \_\_\_\_\_. [ ]  
A) Hit rate B) Miss rate C) Success rate D) Access rate
10. The algorithm which replaces the block which has not been referenced for awhile is called [ ]  
A) LRU B) ORF C) Direct D) Both a and b
  
- 11 . Resource Conflicts can be avoided by using \_\_\_\_\_ [ ]  
A) Single memory space B) Multiple Processors C) Separate instruction & data memories D) All
- 12..In synchronous bus one data transfer in one bus cycle (TRUE/FALSE)
- 13..In synchronous bus data transfer controlled by handshake signals (TRUE/FALSE)
14. Generally processor is the bus master \_\_\_\_\_ (TRUE/FALSE)
- 15..In pipelining the instructions are executed in parallel TRUE/FALSE)
  
16. Data hazard is overcome by using\_\_\_\_\_

- 17..PCI stands for\_\_\_\_\_
- 18.. UMA means\_\_\_\_\_
- 19.Define STATIC RAM\_\_\_\_\_
20. Define pipelining \_\_\_\_\_

- 11 . Resource Conflicts can be avoided by using \_\_\_\_\_ [ ]
- A) Single memory space B) Multiple Processors C) Separate instruction & data memories D) All
- 12..In synchronous bus one data transfer in one bus cycle (TRUE/FALSE)
- 13..In synchronous bus data transfer controlled by handshake signals (TRUE/FALSE)
14. Generally processor is the bus master \_\_\_\_\_ (TRUE/FALSE)
- 15..In pipelining the instructions are executed in parallel TRUE/FALSE)

16. Data hazard is overcome by using\_\_\_\_\_
- 17..PCI stands for\_\_\_\_\_
- 18.. UMA means\_\_\_\_\_
- 19.Define STATIC RAM\_\_\_\_\_
20. Define pipelining \_\_\_\_\_



**G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) KURNOOL**

**IIB.Tech II-SEM OBJECTIVE II-MID EXAM CSE**

**Sub: CO  
10 -05- 17**

**Date:**

**Time: 20 minutes**  
**Max.Marks:10**

**Roll NO:**  
**Invigilator:**

**Signature of**

---

**Answer all the bits, each bit carries ½ mark.**

1. Cache memory works on the principle of \_\_\_\_\_. [ ]  
a).Locality of data b)Locality of memory c) Locality of reference d) none
2. Write Through technique is used in which memory for updating the data \_\_\_\_\_. [ ]  
a)Virtual memoryb)Main memory c)Auxiliary memory d)Cache memory
3. \_\_\_\_\_ is generally used to increase the apparent size of physical memory. [ ]  
a) Secondary memory b) Virtual memory c) Hard-disk d) Disks
4. When the processor receives the request from a device, it responds by sending \_\_\_\_\_. [ ]  
a) Acknowledge signal b) BUS grant signal c) Response signal d) None of the above
5. What characteristic of RAM memory makes it not suitable for permanent storage? [ ]  
a) too slow b)unreliable c) it is volatile d)too bulky
6. Which memory device is generally made of semi-conductors? [ ]  
a) RAM b) Hard-disk c) Floppy disk d) Cd disk
7. The DMA technique where the controller is given complete access to main memory is.... [ ]  
a) Cycle stealing b) Memory stealing c) Memory mode d) Burst mode
8. The DMA controller has \_\_\_\_\_ registers [ ]  
A) 4 B) 2 C) 3 D) 1
9. The algorithm which replaces the block which has not been referenced for awhile is called [ ]  
A) LRU B) ORF C) Direct D) Both a and b
- 10.The number successful accesses to memory stated as a fraction is called as \_\_\_\_\_. [ ]  
A) Hit rate B) Miss rate C) Success rate D) Access rate



**G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) KURNOOL**

**IIB.Tech II-SEM OBJECTIVE II-MID EXAM CSE**

**Sub: CO**  
**10 -05- 17**

**Date:**

**Time: 20 minutes**  
**Max.Marks:10**

**Roll NO:**  
**Invigilator:**

**Signature of**

---

**Answer all the bits, each bit carries ½ mark.**

1. Cache memory works on the principle of \_\_\_\_\_. [ ]  
a).Locality of data b)Locality of memory c) Locality of reference d) none
2. Write Through technique is used in which memory for updating the data \_\_\_\_\_. [ ]  
a)Virtual memoryb)Main memory c)Auxiliary memory d)Cache memory
3. \_\_\_\_\_ is generally used to increase the apparent size of physical memory. [ ]  
a) Secondary memory b) Virtual memory c) Hard-disk d) Disks
4. When the processor receives the request from a device, it responds by sending \_\_\_\_\_. [ ]  
a) Acknowledge signal b) BUS grant signal c) Response signal d) None of the above
5. What characteristic of RAM memory makes it not suitable for permanent storage? [ ]  
a) too slow b)unreliable c) it is volatile d)too bulky

6. Which memory device is generally made of semi-conductors? [ ]  
 a) RAM b) Hard-disk c) Floppy disk d) Cd disk
7. The DMA technique where the controller is given complete access to main memory is... [ ]  
 a) Cycle stealing b) Memory stealing c) Memory mode d) Burst mode
8. The DMA controller has \_\_\_\_\_ registers [ ]  
 A) 4 B) 2 C) 3 D) 1
9. The algorithm which replaces the block which has not been referenced for awhile is called [ ]  
 A) LRU B) ORF C) Direct D) Both a and b
10. The number successful accesses to memory stated as a fraction is called as \_\_\_\_\_ [ ]  
 A) Hit rate B) Miss rate C) Success rate D) Access rate
- 11 . Resource Conflicts can be avoided by using \_\_\_\_\_ [ ]  
 A) Single memory space B) Multiple Processors C) Separate instruction & data memories D) All
12. Generally processor is the bus master \_\_\_\_\_ (TRUE/FALSE)
- 13..In pipelining the instructions are executed in parallel TRUE/FALSE)
14. Data hazard is overcome by using\_\_\_\_\_
- 15...PCI stands for\_\_\_\_\_
- 16.. UMA means\_\_\_\_\_
- 17..In synchronous bus one data transfer in one bus cycle (TRUE/FALSE)
- 18..In synchronous bus data transfer controlled by handshake signals (TRUE/FALSE)
19. Define STATIC RAM\_\_\_\_\_
20. Define pipelining \_\_\_\_\_

- 11 . Resource Conflicts can be avoided by using \_\_\_\_\_ [ ]  
 A) Single memory space B) Multiple Processors C) Separate instruction & data memories D) All
12. Generally processor is the bus master \_\_\_\_\_ (TRUE/FALSE)
- 13..In pipelining the instructions are executed in parallel TRUE/FALSE)
14. Data hazard is overcome by using\_\_\_\_\_

- 15...PCI stands for\_\_\_\_\_
- 16.. UMA means\_\_\_\_\_
- 17..In synchronous bus one data transfer in one bus cycle (TRUE/FALSE)
- 18..In synchronous bus data transfer controlled by handshake signals (TRUE/FALSE)
19. Define STATIC RAM\_\_\_\_\_
20. Define pipelining \_\_\_\_\_



**G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) KURNOOL**

**IIB.Tech II-SEM OBJECTIVE II-MID EXAM CSE**

**Sub: CO  
10 -05-17**

**Date:**

**Time: 20 minutes  
Max.Marks:10**

**Roll NO:  
Invigilator:**

**Signature of**

**Answer all the bits, each bit carries ½ mark.**

1. Write Through technique is used in which memory for updating the data \_\_\_\_\_. [ ]  
a)Virtual memory b)Main memory c)Auxiliary memory d)Cache memory
2. Cache memory works on the principle of \_\_\_\_\_. [ ]  
a).Locality of data b)Locality of memory c) Locality of reference d) none
- 3.\_\_\_\_\_ is generally used to increase the apparent size of physical memory. [ ]  
a) Secondary memory b) Virtual memory c) Hard-disk d) Disks
4. When the processor receives the request from a device, it responds by sending \_\_\_\_\_. [ ]  
a) Acknowledge signal b) BUS grant signal c) Response signal d) None of the above
5. Which memory device is generally made of semi-conductors? [ ]  
a) RAM b) Hard-disk c) Floppy disk d) Cd disk
6. What characteristic of RAM memory makes it not suitable for permanent storage? [ ]  
a) too slow b)unreliable c) it is volatile d)too bulky
7. The DMA technique where the controller is given complete access to main memory is.... [ ]  
a) Cycle stealing b) Memory stealing c) Memory mode d) Burst mode
8. The DMA controller has \_\_\_\_\_ registers [ ]  
A) 4 B) 2 C) 3 D) 1
9. The algorithm which replaces the block which has not been referenced for awhile is called [ ]  
A) LRU B) ORF C) Direct D) Both a and b
- 10.The number successful accesses to memory stated as a fraction is called as \_\_\_\_\_. [ ]  
A) Hit rate B) Miss rate C) Success rate D) Access rate



**G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) KURNOOL**

**IIB.Tech II-SEM OBJECTIVE II-MID EXAM CSE**

Time: 20 minutes  
Max.Marks:10

Roll NO:  
Invigilator:

Signature of

---

Answer all the bits, each bit carries ½ mark.

1. Write Through technique is used in which memory for updating the data \_\_\_\_\_. [ ]  
a)Virtual memory b)Main memory c)Auxiliary memory d)Cache memory
2. Cache memory works on the principle of \_\_\_\_\_. [ ]  
a).Locality of data b)Locality of memory c) Locality of reference d) none
3. \_\_\_\_\_ is generally used to increase the apparent size of physical memory. [ ]  
a) Secondary memory b) Virtual memory c) Hard-disk d) Disks
4. When the processor receives the request from a device, it responds by sending \_\_\_\_\_. [ ]  
a) Acknowledge signal b) BUS grant signal c) Response signal d) None of the above
5. Which memory device is generally made of semi-conductors? [ ]  
a) RAM b) Hard-disk c) Floppy disk d) Cd disk
6. What characteristic of RAM memory makes it not suitable for permanent storage? [ ]  
a) too slow b)unreliable c) it is volatile d)too bulky
7. The DMA technique where the controller is given complete access to main memory is.... [ ]  
a) Cycle stealing b) Memory stealing c) Memory mode d) Burst mode
8. The DMA controller has \_\_\_\_\_ registers [ ]  
A) 4 B) 2 C) 3 D) 1
9. The algorithm which replaces the block which has not been referenced for awhile is called [ ]  
A) LRU B) ORF C) Direct D) Both a and b
- 10.The number successful accesses to memory stated as a fraction is called as \_\_\_\_\_ [ ]  
A) Hit rate B) Miss rate C) Success rate D) Access rate
  
- 11) . Resource Conflicts can be avoided by using \_\_\_\_\_ [ ]  
A) Single memory space B) Multiple Processors C) Separate instruction & data memories D) All
- 12.Generally processor is the bus master \_\_\_\_\_ (TRUE/FALSE)
- 13.In pipelining the instructions are executed in parallel \_\_\_\_\_ (TRUE/FALSE)
- 14.In synchronous bus one data transfer in one bus cycle \_\_\_\_\_ (TRUE/FALSE)
- 15.In synchronous bus data transfer controlled by handshake signals (TRUE/FALSE)
16. Data hazard is overcome by using \_\_\_\_\_
- 17..PCI stands for \_\_\_\_\_
- 18.. UMA means \_\_\_\_\_
- 19.Define STATIC RAM \_\_\_\_\_
20. Define pipelining \_\_\_\_\_

- 11) . Resource Conflicts can be avoided by using \_\_\_\_\_ [ ]  
A) Single memory space B) Multiple Processors C) Separate instruction & data memories D) All
12. Generally processor is the bus master \_\_\_\_\_ (TRUE/FALSE)
13. In pipelining the instructions are executed in parallel \_\_\_\_\_ (TRUE/FALSE)
14. In synchronous bus one data transfer in one bus cycle \_\_\_\_\_ (TRUE/FALSE)
15. In synchronous bus data transfer controlled by handshake signals (TRUE/FALSE)
16. Data hazard is overcome by using \_\_\_\_\_
17. PCI stands for \_\_\_\_\_
18. UMA means \_\_\_\_\_
19. Define STATIC RAM \_\_\_\_\_
20. Define pipelining \_\_\_\_\_