G. PULLAIAH COLLEGE OF ENGINEERING AND TECHNOLOGY

Accredited by NAAC with 'A' Grade of UGC, Approved by AICTE, New Delhi

Permanently Affiliated to JNTUA, Ananthapuramu

(Recognized by UGC under 2(f) and 12(B) & ISO 9001:2008 Certified Institution)

Nandikotkur Road, Venkayapalli, Kurnool – 518452

Department of Electronics and Communication Engineering

Bridge Course
On

Linear IC Applications

Linear IC Applications

DIFFERENTIAL AMPLILFIER:

Let us consider the emitter biased circuit. Below figure 1.1(a) shows two identical emitter biased circuits that transistor Q_1 has the same characteristics as the transistor Q_2. $R_{E1} = R_{E2}$, and the magnitudes of $+V_{CC} = -V_{EE}$

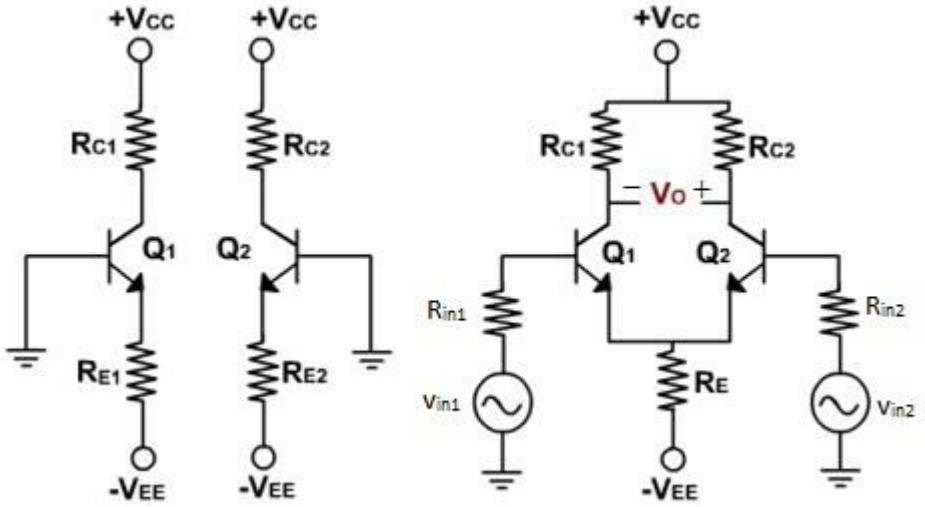


Figure 1.1 (a) : Two identical emitter biased circuits (b) Dual input, balanced output differential amplifier.

To obtain a single circuit such as the one in figure 1.1(b) we should reconnect these two circuits as follows:

1. Reconnect $+V_{CC}$ and $-V_{EE}$ supply voltages of the two circuits, since voltages are of the same polarity and amplitudes.
2. Reconnect the emitter E_1 of transistor Q_1 to the emitter E_2 of transistor Q_2. (This reconnection replaces R_{E1} in parallel with R_{E2}).
3. Show the input signal v_{in1} applied to the base B_1 of transistor Q_1 and v_{in2} applied to the base B_2 of transistor Q_2.
4. Label the voltage between the collectors C_1 and C_2 as v_o. (the v_o is the output voltage.)

The circuit of figure 1.1(b) depicts these changes and is referred to as a differential amplifier.

The differential amplifier of figure 1.1(b), amplifies the difference between two input signal v_{in1} and v_{in2}. (The differential amplifier is also referred to as difference amplifier).

DIFFERENTIAL AMPLIFIER CONFIGURATIONS:

The four differential amplifier configurations are the following:

1. Dual–input, balanced–output differential amplifier.
2. Dual–input, unbalanced–output differential amplifier.
3. Single–input, balanced–output differential amplifier.
4. Single–input, unbalanced–output differential amplifier.

The configurations listed are defined by the number of input signals used and the way an output voltage is measured.

If we use two input signals, the configuration is said to be dual input, otherwise it is single input configuration.

On the other hand, if the output is measured between two collectors, it is referred to as balanced output because both collectors are at the same dc potential with respect to ground. However, if the output is measured at one of the collectors with respect to ground, the configuration is called an unbalanced output.

Some general observations on differential amplifier are as follows:

- ✓ Two matched semiconductors of the same type (BJT's or FET's)
- ✓ All the components must be matched in all respects for proper operation.
- ✓ The magnitude of the supply voltages $+V_{CC}$ and $-V_{EE}$ must be equal.

DUAL INPUT, BALANCED OUTPUT DIFFERENTIAL AMPLIFIER:

The circuit shown in figure 1.1(b) is a dual input, balanced output differential amplifier. The two input signals (dual input), v_{in1} and v_{in2}, are applied to the bases B_1 and B_2 of transistors Q_1 and Q_2. The output v_o is measured between the two collectors, C_1 and C_2 which are at the same dc potential. Because of the equal dc potential at the two collectors with respect to ground the output is referred to as a balanced output.

DC Analysis: To determine the operating point values (I_{cQ} and V_{CEQ}) for the differential amplifier of figure 1.1(b), we need to obtain a dc equivalent circuit.

The dc equivalent circuit can be obtained simply by reducing the input signal v_{in1} and v_{in2} to zero. The dc equivalent circuit that obtained is shown in figure 1.2. Note that the internal resistances of the input signals are denoted by R_{in1} because $R_{in1} = R_{in2}$. Since both the emitter – biased sections of the differential amplifier are symmetry (matched in all respects), we need to determine the operating point (I_{CQ} and V_{CEQ}) for only one section.

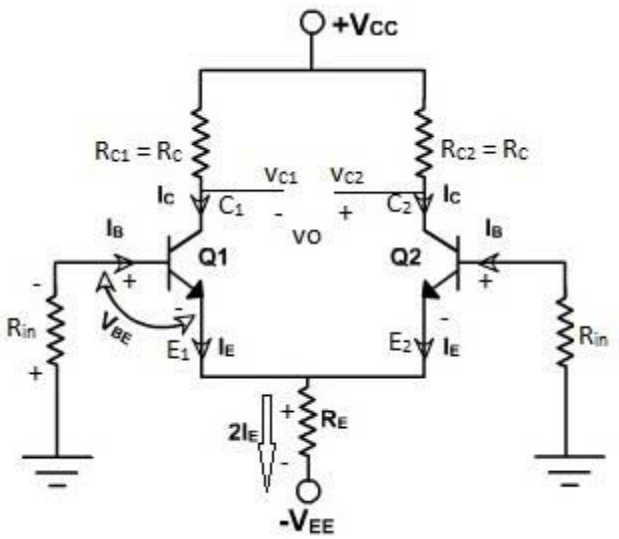


Figure 1.2 : DC equivalent circuit of the dual – input, balanced – output differential amplifier.

We shell determine the I_{cQ} and V_{CEQ} values can then be used for transistor Q_1 only. These I_{cQ} and V_{CEQ} values can then be used for transistor Q_2 also.

Applying KVL to the base – emitter loop of the transistor Q_1

$$-R_{in} I_B - V_{BE} - R_E (2I_E) + V_{EE} = 0 \qquad \text{------> (1.1)}$$

But $I_B = \frac{I_E}{\beta_{dc}}$ since $I_C \cong I_E$

Hence $-R_{in} (\frac{I_E}{\beta_{dc}}) - V_{BE} - R_E (2I_E) + V_{EE} = 0$

$$\Rightarrow \boxed{I_E = I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_{in}}{\beta_{dc}}}} \quad \text{------> (1.2)}$$

Where V_{BE} = 0.6 V for Si transistors.
= 0.2 V for Ge transistors.

Generally $\frac{R_{in}}{\beta_{dc}} \ll 2R_E$

$$\therefore \boxed{I_E = I_{CQ} \cong \frac{V_{EE} - V_{BE}}{2R_E}} \quad \text{------> (1.3)}$$

From the equation (1.3) we see that the value of R_E sets up the I_E in transistors Q_1 and Q_2 for given values of V_{EE}. In other words, by selecting a desired value of emitter - V_{EE}.

Note: I_E in transistors Q_1 and Q_2 is independent of collector resistance R_C.

To determine V_{CEQ} , $V_{CE} = V_C - V_E$

The voltage at the emitter of transistor Q_1 is approximately equal to $-V_{BE}$ if we assume the voltage drop across the R_{in} to be negligible small. (i.e $V_E = -V_{BE}$) knowing the value of I_E ($\cong I_C$), we can obtain the voltage at the collector V_C, as

$V_c = V_{CC} - I_C R_C$

Thus the $V_{CE} = V_C - V_E$

$= V_{CC} - I_C R_C - (- V_{BE})$

$= V_{CC} + V_{BE} - I_C R_C$

$$\boxed{V_{CE} = V_{CC} + V_{BE} - I_C R_C} \quad \text{------> (1.4)}$$

At the operating point $I_E = I_{CQ}$ and $V_{CE} = V_{CEQ}$ thus we can determine operating point I_{CQ} and V_{CEQ} by using equations (1.3) and (1.4) respectively.

Note : The dc analysis equations (1.2) and (1.4) are applicable for all four differential amplifier configuration as long as we use the same biasing arrangement for each of them.

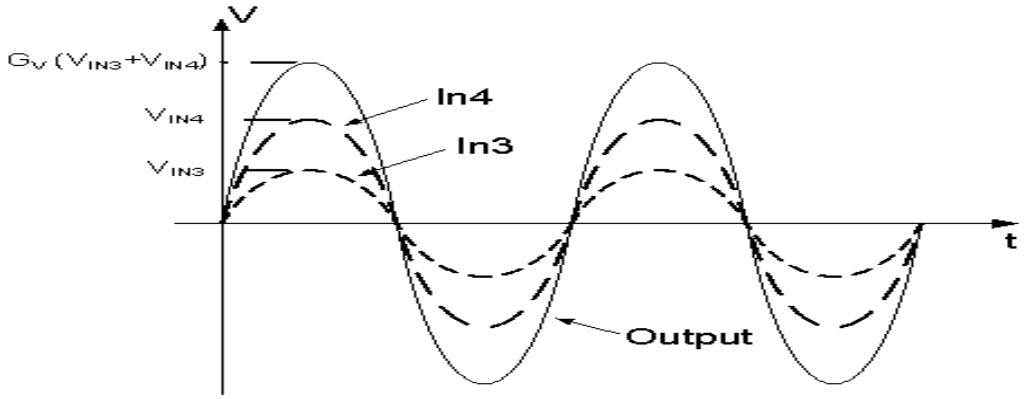
AC ANALYSIS: To perform ac analysis to derive the expression for the voltage gain A_d, and the input resistance R_i of the differential amplifier shown in figure 1.3(a).

1. Set the dc voltages + V_{CC} and -V_{EE} at zero.
2. Substitute the small signal T – equivalent models for the transistors.

Figure 1.3(a) shows the resulting ac equivalent circuit of the dual – input, balanced – output differential amplifier.

(a) Voltage gain (A_d): some general observations on ac equivalent circuit are as follows

1. $I_{E1} = I_{E2}$; therefore $r_{e1} = r_{e2} = r_e$.
2. The voltage across each collector resistor is show out of phase by 180^0 with respect to input voltages v_{in1} and v_{in2}
3. The polarity of output voltage (v_o), simply indicates that the voltage at collector C_2 is assumed to be more positive with respect to that at collector C_1, even though both of them are negative with respect to ground.



(a) AC equivalent circuit *(b) Input and output waveforms.*

Figure 1.3 Dual – input, balanced – output Differential amplifier

Writing KVL equations for loops I and II in figure 1.3 (a)

$v_{in1} - R_{in1}\, i_{b1} - r_e\, i_{e1} - R_E(\, i_{e1} + i_{e2}\,) = 0$ ------> (1.5)

$v_{in2} - R_{in2}\, i_{b2} - r_e\, i_{e2} - R_E(\, i_{e1} + i_{e2}\,) = 0$ ------> (1.6)

We know that $i_{b1} = \frac{i_{e1}}{\beta_{ac}}$ *and* $i_{b2} = \frac{i_{e2}}{\beta_{ac}}$

$v_{in1} - \frac{R_{in1}}{\beta_{ac}}\, i_{e1} - r_e\, i_{e1} - R_E(\, i_{e1} + i_{e2}\,) = 0$

$v_{in2} - \frac{R_{in2}}{\beta_{ac}}\, i_{e2} - r_e\, i_{e2} - R_E(\, i_{e1} + i_{e2}\,) = 0$

generally, $\frac{R_{in1}}{\beta_{ac}}$ and $\frac{R_{in2}}{\beta_{ac}}$ are very small; there we shell neglect here for simplicity. Hence

$(r_e + R_E)\, i_{e1} + R_E\, i_{e2} = v_{in1}$ ------> (1.7)

$R_E\, i_{e1} + (r_e + R_E)\, i_{e2} = v_{in2}$ ------> (1.8)

Using Cramer's rule:

$$i_{e1} = \frac{\begin{vmatrix} v_{in1} & R_E \\ v_{in2} & r_e + R_E \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}}$$

$$= \frac{(r_e + R_E)v_{in1} - R_E\, v_{in2}}{(r_e + R_E)^2 - {R_E}^2} \quad \text{------> (1.9a)}$$

$$i_{e2} = \frac{\begin{vmatrix} r_e + R_E & v_{in1} \\ R_E & v_{in2} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}}$$

$$= \frac{(r_e + R_E)v_{in2} - R_E\, v_{in1}}{(r_e + R_E)^2 - {R_E}^2} \quad \text{------> (1.9b)}$$

The output voltage is, $v_o = v_{c2} - v_{c1}$

$= - R_C \,.\, i_{C2} - (- R_C.i_{C1})$

$= R_C \,.\, i_{C1} - R_C.i_{C2}$

$= R_C\, (\, i_{e1} - i_{e2}\,)$ since $i_C \cong i_e$ ------> (1.10)

Substituting equations (1.9a) and (1.9b) in equation (1.10)

$$v_o = R_C \left[\frac{(r_e + R_E)v_{in1} - R_E\, v_{in2}}{(r_e + R_E)^2 - {R_E}^2} - \frac{(r_e + R_E)v_{in2} - R_E\, v_{in1}}{(r_e + R_E)^2 - {R_E}^2} \right]$$

$$= R_C \left[\frac{(r_e + R_E)(\, v_{in1} - v_{in2}) - R_E\, (v_{in1} - v_{in2})}{(r_e + R_E)^2 - {R_E}^2} \right]$$

$$= R_C \left[\frac{(r_e + 2R_E)(v_{in1} - v_{in2})}{r_e^2 + 2r_e R_E} \right]$$

$$= \frac{R_C}{r_e} (v_{in1} - v_{in2}) \quad \text{------> (1.11)}$$

Thus a differential amplifier amplifies the difference between two input signals.

Figure 1.3(b) shows the input and output waveforms of the dual input, balanced output differential amplifier.

By defining $v_{id} = v_{in1} - v_{in2}$

Voltage gain $\boxed{A_d = \frac{v_o}{v_{id}} = \frac{R_C}{r_e}}$ ------> (1.12)

Note: i) A_d independent on R_E

ii) Identical to the voltage gain equation of CE amplifier.

(b) Differential Input Resistance (R_{i1} or R_{i2}):

Differential input resistance is defined as the equivalent resistance that would be measured at either input terminal with the other input terminal grounded.

i.e the input resistance R_{i1} seen from the input signal source v_{in1} is determined with the signal source v_{in2} set at zero.

Similarly, the input signal source v_{in1} set at zero to determine the input resistance R_{i2} seen from the input signal source v_{in2}.

See figure 1.3(a), R_{in1} and R_{in2} are very small and hence will be ignored in the derivation of input resistances R_{i1} and R_{i2}

$$R_{i1} = \left| \frac{v_{in1}}{i_{b1}} \right|_{/v_{in2}=0} = \left| \frac{v_{in1}}{i_{e1}/\beta_{ac}} \right|_{/v_{in2}=0}$$

Substituting equation (1.9a), we get

$$R_{i1} = \frac{\beta_{ac} v_{in1}}{\frac{(r_e + R_E) v_{in1} - R_E (0)}{(r_e + R_E)^2 - R_E^2}}$$

$$= \frac{\beta_{ac} (r_e^2 + 2r_e R_E)}{r_e + R_E}$$

$$R_{i1} = \frac{\beta_{ac} r_e (r_e + 2R_E)}{r_e + R_E} \quad \text{------> (1.13)}$$

Generally $R_E >> r_e$ $\Rightarrow$ $(r_e + 2R_E) \cong 2R_E$ *and* $(r_e + R_E) \cong R_E$ hence equation 1.13 can be written as

$$R_{i1} = \frac{\beta_{ac} r_e . 2R_E}{R_E}$$

$$\boxed{R_{i1} = 2\beta_{ac} r_e} \quad \text{------> (1.14)}$$

Similarly the input resistance R_{i2} from the input signal source v_{in2} is defined as:

$$R_{i2} = \left| \frac{v_{in2}}{i_{b2}} \right|_{/v_{in1}=0} = \left| \frac{v_{in2}}{i_{e2}/\beta_{ac}} \right|_{/v_{in1}=0}$$

Substitute equation (1.9b), we obtain

$$R_{i2} = \frac{\beta_{ac} v_{in2}}{\frac{(r_e + R_E) v_{in2} - R_E (0)}{(r_e + R_E)^2 - R_E^2}}$$

$$= \frac{\beta_{ac} (r_e^2 + 2r_e R_E)}{r_e + R_E}$$

$$R_{i2} = \frac{\beta_{ac} r_e (r_e + 2R_E)}{r_e + R_E} \quad \text{------> (1.15)}$$

However $R_E >> r_e$ $\Rightarrow$ $(r_e + 2R_E) \cong 2R_E$ *and* $(r_e + R_E) \cong R_E$ hence equation 1.15 can be written as

$$R_{i2} = \frac{\beta_{ac}\, r_e . 2R_E}{R_E}$$

$$\boxed{R_{i2} = 2\beta_{ac}\, r_e} \quad \text{------> (1.16)}$$

(c) Output Resistance (R_o): Output resistance is defined as the equivalent resistance that would be measured at either output terminal (C_1 or C_2) with respect to ground.

Therefore, the output resistance R_{o1} measured between collector C_1 and ground is equal to that of the collector resistor R_C [see figure 1.3(a)].

Similarly the output resistance R_{o2} measured at collector C_2 with respect to ground is equal to that of the collector resistance R_C. Thus $\boxed{R_{o1} = R_{o2} = R_C}$ ------> (1.17)

*Note: The current gain of the differential amplifier is undefined; therefore the current gain equation will not be derived for any of the four differential amplifier configurations.

Furthermore, like the CE amplifier the differential amplifier is a small signal amplifier therefore, it is generally used as voltage amplifier and not a current or power amplifier.

Inverting and Non – inverting input terminals : In the differential amplifier circuit of figure 1.2 the input voltage v_{in1} is called the non – inverting input, similarly the input voltage v_{in2} is called the inverting input.

Consequently, the base terminal B_1 to which v_{in1} is applied is referred to as the non – inverting input terminal and the base terminal B_2 is called the inverting input terminal.

Common Mode Rejection Ratio (CMRR): An important characteristic of the dual-input balanced output differential amplifier is its ability to suppress undesired disturbances that might be amplified along with the desired signal.

When the matched pair of transistors is used in the differential amplifier, the unwanted signals, such as 60 – Hz noise or hum pick–up would appear as common to both input bases, and therefore the net output would theoretically be zero.

The practical effectiveness of rejecting the common signal, depends on the degree of matching between the two common–emitter stages forming the differential amplifier.

In otherwards, more closely equal are the currents in the input transistors Q_1 and Q_2 the better is the common mode signal rejection (see figure 1.4). When the same voltage is applied to both input terminals of a differential amplifier, the differential amplifier is said to be operate in the common mode configuration.

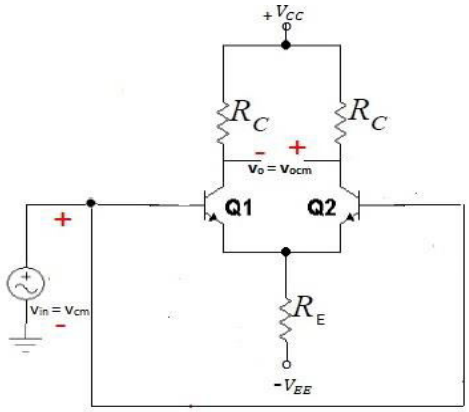


Figure 1.4 Differential amplifier in common–mode configuration.

The ability of a differential amplifier to reject a common mode signal is expressed by its CMRR. It is the ratio of differential gain (A_d) to the common-mode gain (A_{cm}). In equation form

$$\boxed{CMRR = \frac{A_d}{A_{cm}}} \quad \text{------> (1.18)}$$

A common mode voltage gain A_{cm} can be determined as follows:

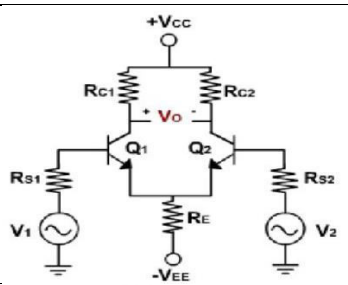
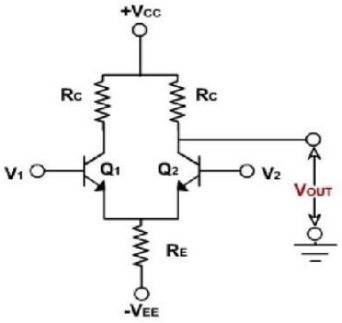
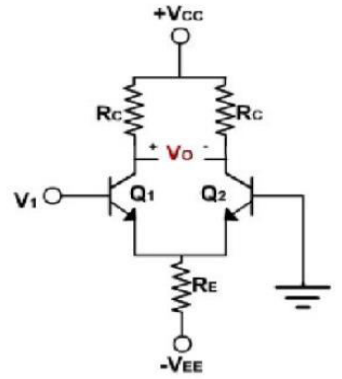
- Apply a known voltage v_{cm} to both input terminals of the differential amplifier as shown in the above (figure 1.4)
- Measure the resultant output voltage v_{ocm}. Then calculate

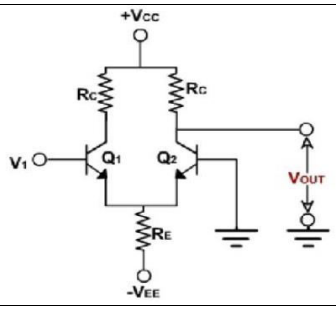
$$\boxed{A_{cm} = \frac{v_{ocm}}{v_{cm}}} \quad \text{------> (1.19)}$$

- Ideally we expect A_{cm} to be zero, i.e. $v_{ocm} = 0$

The properties of the four types of differential amplifiers discussed are summarized in Table 1.1.

TABLE 1.1 PROPERTIES OF THE DIFFERENTIAL AMPLIFIER CIRCUIT CONFIGURATIONS

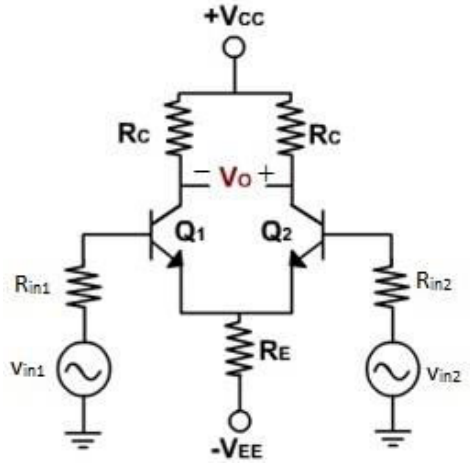
Configurations	Circuit	Voltage gain	Input resistance	Output resistance
1. Dual Input, Balanced Output		$A_d = \frac{R_C}{r_e}$	$R_{i1} = 2\beta_{ac}r_e$ $R_{i2} = 2\beta_{ac}r_e$	$R_{o1} = R_C$ $R_{o2} = R_C$
2. Dual-Input, Unbalanced Output		$A_d = \frac{R_C}{2r_e}$	$R_{i1} = 2\beta_{ac}r_e$ $R_{i2} = 2\beta_{ac}r_e$	$R_o = R_C$
3. Single Input, Balanced Output		$A_d = \frac{R_C}{r_e}$	$R_i = 2\beta_{ac}r_e$	$R_{o1} = R_C$ $R_{o2} = R_C$

4. Single-Input, Unbalanced Output		$A_d = \frac{R_C}{2r_e}$	$R_i = 2\beta_{ac}r_e$	$R_o = R_C$

Problem 1.1: The following specifications are given for the dual-input, balanced-output differential amplifier of figure (1.1): R_C = 2.2 kΩ, R_C = 2.2 kΩ, R_E = 4.7 kΩ, $R_{in1} = R_{in2}$ = 50 Ω, + V_{CC} = + 10V, - V_{EE} = -10V and the transistor is the CA3086 with $\beta_{ac} = \beta_{dc}$ =100 and V_{BE} = 0.715V typical.

(a) Determine the I_{CQ} and V_{CEQ} values. (b) Determine the voltage gain.

(c) Determine the input and output resistances.



Solution: (a) To determine I_{CQ} and V_{CQ} values, we have to substitute the known values in equations (1.2 & 1.4) as follow:

$$I_E = I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_{in}}{\beta_{dc}}} = \frac{10-0.715}{94+\frac{50}{100}} = 0.988\ mA$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$

= 10 + 0.715 – (2.2 kΩ)(0.988 mA)

= 8.54 V

(a) The ac emitter resistance: $r_e = \frac{25\ mV}{I_E\ mA} = \frac{25\ mV}{0.988\ mA} = 25.3\ \Omega$

Therefore substituting the known values in the voltage-gain equation (1.12), we obtain

$$A_d = \frac{v_o}{v_{id}} = \frac{R_C}{r_e} = \frac{2200}{25.3} = 86.96$$

(b) The input resistance seen from each input source is given by equation (1.14 & 1.15)

$$R_{i1} = R_{i2} = 2\beta_{ac}\, r_e = (2)(100)(25.3) = 5.06\ k\Omega$$

The output resistance seen looking back into the circuit from each of the two output terminals is given by equation (1.17): $R_{o1} = R_{o2} = R_C = 2.2\ k\Omega$

Digital IC Applications

COMBINATIONAL CIRCUITS:

Logic circuits for digital systems may be combinational or sequential. The output of a combinational circuit depends on its present inputs only .Combinational circuit processing operation fully specified logically by a set of Boolean functions .A combinational circuit consists of input variables, logic gates and output variables.Both input and output data are represented by signals, i.e., they exists in two possible values. One is logic –1 and the other logic 0.

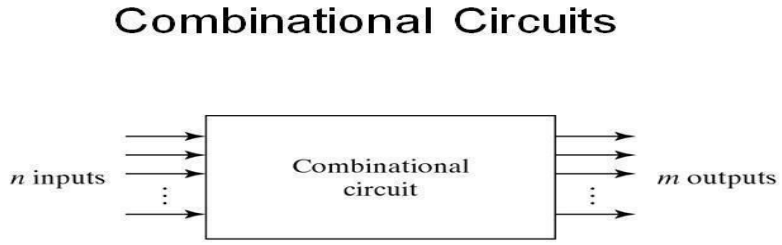


Fig. Block Diagram of Combinational Circuit

For n input variables,there are 2^n possible combinations of binary input variables .For each possible input Combination ,there is one and only one possible output combination.A combinational circuit can be described by m Boolean functions one for each output variables.Usually the input s comes from flip-flops and outputs goto flip-flops.

Adders:

Digital computers perform variety of information processing tasks,the one is arithmetic operations.And the most basic arithmetic operation is the addition of two binary digits.i.e, 4 basic possible operations are:

0+0=0,0+1=1,1+0=1,1+1=10

The first three operations produce a sum whose length is one digit, but when augends and addend bits are equal to 1,the binary sum consists of two digits.The higher significant bit of this result is called a carry.A combinational circuit that performs the addition of two bits is called a half-adder. One that performs the addition of 3 bits (two significant bits & previous carry) is called a full adder.& 2 half adder can employ as a full-adder.

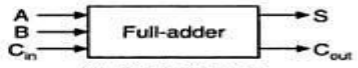
The Full Adder:

A Full-adder is a combinational circuit that adds two bits and a carry and outputs a sum bit and a carry bit. To add two binary numbers, each having two or more bits, the LSBs can be added by using a half-adder. The carry resulted from the addition of the LSBs is carried over to the next significant column and added to the two bits in that column. So, in the second and higher columns, the two data bits of that column and the carry bit generated from the addition in the previous column need to be added.

The full-adder adds the bits A and B and the carry from the previous column called the carry-in C_{in} and outputs the sum bit S and the carry bit called the carry-out C_{out} . The variable S gives the value of the least significant bit of the sum. The variable C_{out} gives the output carry.The eight rows under the input variables designate all possible combinations of 1s and 0s that these variables may have. The 1s and 0s for the output variables are determined from the arithmetic sum of the input bits. When all the bits are 0s , the output is 0. The S output is equal to 1 when only 1 input is equal to 1 or when all the inputs are equal to 1. The C_{out} has a carry of 1 if two or three inputs are equal to 1.

Inputs			Sum	Carry
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a) Truth table



(b) Block diagram

Full-adder.

From the truth table, a circuit that will produce the correct sum and carry bits in response to every possible combination of A,B and C_{in} is described by

$$S = \overline{A}\,\overline{B}C_{in} + A\overline{B}\,\overline{C_{in}} + AB\overline{C_{in}} + ABC_{in}$$

$$C_{out}$$

$$= \overline{A}BC_{in} + AB\overline{C_{in}} + ABC_{in} + ABC_{in}$$

$$S = A \oplus B \oplus C_{in}$$

$$C_{out} = AC_{in} + BC_{in} + AB$$

Subtractors:

The subtraction of two binary numbers may be accomplished by taking the complement of the subtrahend and adding it to the minuend. By this, the subtraction operation becomes an addition operation and instead of having a separate circuit for subtraction, the adder itself can be used to perform subtraction. In subtraction, each subtrahend bit of the number is subtracted from its corresponding significant minuend bit to form a difference bit.

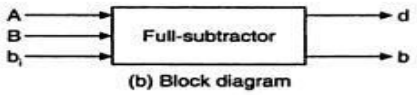
The Full-Subtractor:

The half-subtractor can be only for LSB subtraction. IF there is a borrow during the subtraction of the LSBs, it affects the subtraction in the next higher column; the subtrahend bit is subtracted from the minuend bit, considering the borrow from that column used for the subtraction in the preceding column. Such a subtraction is performed by a full-subtractor. It subtracts one bit (B) from another bit (A) , when already there is a borrow b_i from this column for the subtraction in the preceding column, and outputs the difference bit (d) and the borrow

bit(b) required from the next d and b. The two outputs present the difference and output borrow. The 1s and 0s for the output variables are determined from the subtraction of A-B-b_i.

Inputs			Difference	Borrow
A	B	b_i	d	b
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

(a) Truth table



(b) Block diagram

Full-subtractor.

From the truth table, a circuit that will produce the correct difference and borrow bits in response to every possible combinations of A,B and b_i is

$$d = \bar{A}\bar{B}b_i + \bar{A}B\bar{b}_i + A\bar{B}\bar{b}_i + ABb_i$$
$$= b_i(AB + \bar{A}\bar{B}) + \bar{b}_i(A\bar{B} + \bar{A}B)$$
$$= b_i(\overline{A \oplus B}) + \bar{b}_i(A \oplus B) = A \oplus B \oplus b_i$$

and

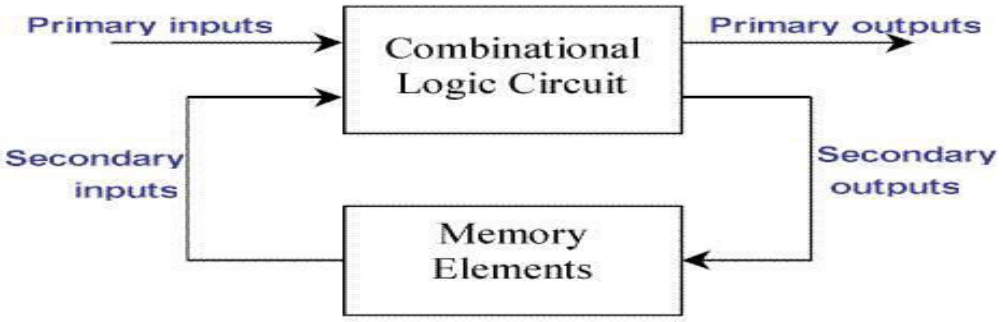
$$b = \bar{A}\bar{B}b_i + \bar{A}B\bar{b}_i + \bar{A}Bb_i + ABb_i = \bar{A}B(b_i + \bar{b}_i) + (AB + \bar{A}\bar{B})b_i$$
$$= \bar{A}B + (\overline{A \oplus B})b_i$$

SEQUENTIAL CIRCUITS:

Classification of sequential circuits: Sequential circuits may be classified as two types.

1. Synchronous sequential circuits
2. Asynchronous sequential circuits

Combinational logic refers to circuits whose output is strictly depended on the present value of the inputs. As soon as inputs are changed, the information about the previous inputs is lost, that is, combinational logics circuits have no memory. Although every digital system is likely to have combinational circuits, most systems encountered in practice also include memory elements, which require that the system be described in terms of sequential logic. Circuits whose output depends not only on the present input value but also the past input value are known as **sequential logic circuits**. The mathematical model of a sequential circuit is usually referred to as a **sequential machine**.



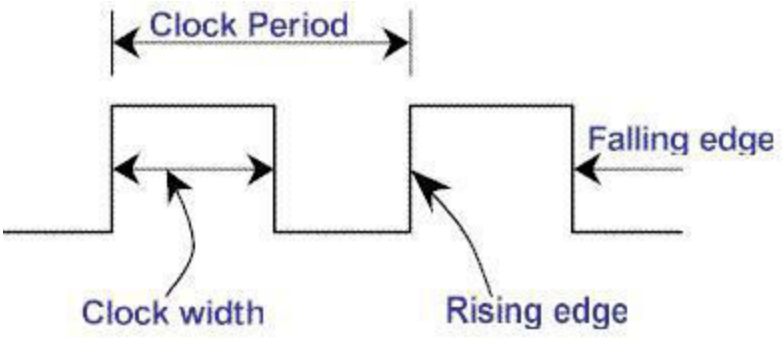
Comparison between combinational and sequential circuits

Combinational circuit	Sequential circuit
1. In combinational circuits, the Output variables at any instant of time are dependent only on the present input variables	1. in sequential circuits the output variables at any instant of time are dependent not only on the present input variables, but also on the present state
2.Memory unit is not requires in combinational circuit	2.Memory unit is required to store the past history of the input variables
3. These circuits are faster because the delay between the i/p and o/p due to propagation delay of gates only	3. Sequential circuits are slower than combinational circuits
4. easy to design	4. comparatively hard to design

There are two types of asynchronous circuits: fundamental mode circuits and pulse mode circuits.

Synchronous and Asynchronous Operation:

Sequential circuits are divided into two main types: **synchronous** and **asynchronous**. Their classification depends on the timing of their signals.***Synchronous*** sequential circuits change their states and output values at discrete instants of time, which are specified by the rising and falling edge of a free-running **clock signal**. The clock signal is generally some form of square wave as shown in Figure below.



From the diagram you can see that the **clock period** is the time between successive transitions in the same direction, that is, between two rising or two falling edges. State transitions in synchronous sequential circuits are made to take place at times when the clock is making a transition from 0 to 1 (rising edge) or from 1 to 0 (falling edge). Between successive clock pulses there is no change in the information stored in memory.

The reciprocal of the clock period is referred to as the **clock frequency**. The **clock width** is defined as the time during which the value of the clock signal is equal to 1. The ratio of the

clock width and clock period is referred to as the duty cycle. A clock signal is said to be **active high** if the state changes occur at the clock's rising edge or during the clock width. Otherwise, the clock is said to be **active low**. Synchronous sequential circuits are also known as **clocked sequential circuits**.

In ***asynchronous*** sequential circuits, the transition from one state to another is initiated by the change in the primary inputs; there is no external synchronization. The memory commonly used in asynchronous sequential circuits are time-delayed devices, usually implemented by feedback among logic gates. Thus, asynchronous sequential circuits may be regarded as combinational circuits with feedback. Because of the feedback among logic gates, asynchronous sequential circuits may, at times, become unstable due to transient conditions. The instability problem imposes many difficulties on the designer. Hence, they are not as commonly used as synchronous systems.

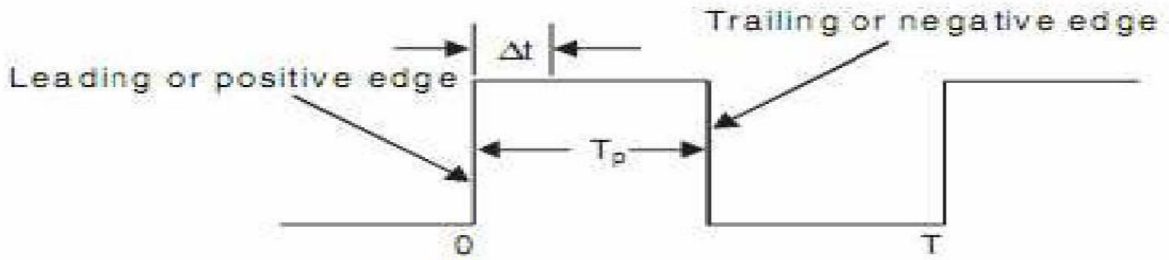
Latches and flip-flops

Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted.

There are basically four main types of latches and flip-flops: SR, D, JK, and T. The major differences in these flip-flop types are the number of inputs they have and how they change state. For each type, there are also different variations that enhance their operations.

Race around Condition

The inherent difficulty of an S-R flip-flop (i.e., S = R = 1) is eliminated by using the feedback connections from the outputs to the inputs of gate 1 and gate 2 as shown in Figure. Truth tables in figure were formed with the assumption that the inputs do not change during the clock pulse (CLK = 1). But the consideration is not true because of the feedback connections



1. Consider, for example, that the inputs are J = K = 1 and Q = 1, and a pulse as shown in Figure is applied at the clock input.
2. After a time interval t equal to the propagation delay through two NAND gates in series, the outputs will change to Q = 0. So now we have J = K = 1 and Q = 0.
3. After another time interval of t the output will change back to Q = 1. Hence, we conclude that for the time duration of tP of the clock pulse, the output will oscillate between 0 and 1. Hence, at the end of the clock pulse, the value of the output is not certain. This situation is referred to as a race-around condition.

- Generally, the propagation delay of TTL gates is of the order of nanoseconds. So if the clock pulse is of the order of microseconds, then the output will change thousands of times within the clock pulse.

1. This race-around condition can be avoided if tp< t < T. Due to the small propagation delay of the ICs it may be difficult to satisfy the above condition.
2. A more practical way to avoid the problem is to use the master-slave (M-S) configuration as discussed below.

Applications of flip-flops:

Frequency Division: When a pulse waveform is applied to the clock input of a J-K flip-flop that is connected to toggle, the Q output is a square wave with half the frequency of the clock input. If more flip-flops are connected together as shown in the figure below, further division of the clock frequency can be achieved

. **Parallel data storage:** a group of flip-flops is called register. To store data of N bits, N flip-flops are required. Since the data is available in parallel form. When a clock pulse is applied to all flip-flops simultaneously, these bits will transfer will be transferred to the Q outputs of the flip flops.

Serial data storage: to store data of N bits available in serial form, N number of D-flip-flops is connected in cascade. The clock signal is connected to all the flip-flops. The serial data is applied to the D input terminal of the first flip-flop.

Shift registers:

In digital circuits, a **shift register** is a cascade of flip-flops sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, *shifting in* the data present at its input and *shifting out* the last bit in the array, at each transition of the clock input. More generally, a **shift register** may be multidimensional, such that its "data in" and stage outputs are themselves bit arrays: this is implemented simply by running several shift registers of the same bit-length in parallel.

Shift registers can have both parallel and serial inputs and outputs. These are often configured as **serial-in, parallel-out** (SIPO) or as **parallel-in, serial-out** (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also **bi-directional** shift registers which allow shifting in both directions: L→R or R→L. The serial input and last output of a shift register can also be connected to create a **circular shift register**

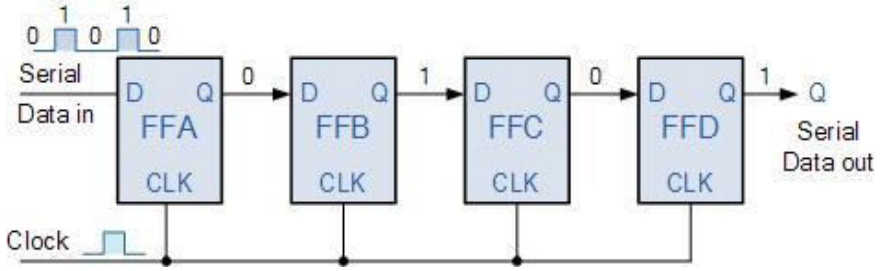
Shift registers are a type of logic circuits closely related to counters. They are basically for the storage and transfer of digital data.

A number of flipflops connected together such that data may be shifted into and shifted out of them is called shift register. data may be shifted into or out of the register in serial form or in parallel form. There are four basic types of shift registers.

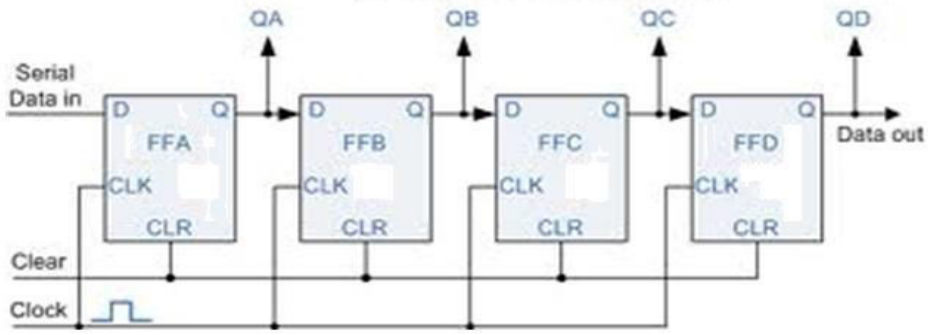
1. Serial in, serial out, shift right, shift registers
2. Serial in, serial out, shift left, shift registers
3. Parallel in, serial out shift registers
4. Parallel in, parallel out shift registers

Serial IN, serial OUT, shift right, shift left register:

The logic diagram of 4-bit serial in serial out, right shift register with four stages. The register can store four bits of data. Serial data is applied at the input D of the first FF. the Q output of the first FF is connected to the D input of another FF. the data is outputted from the Q terminal of the last FF.

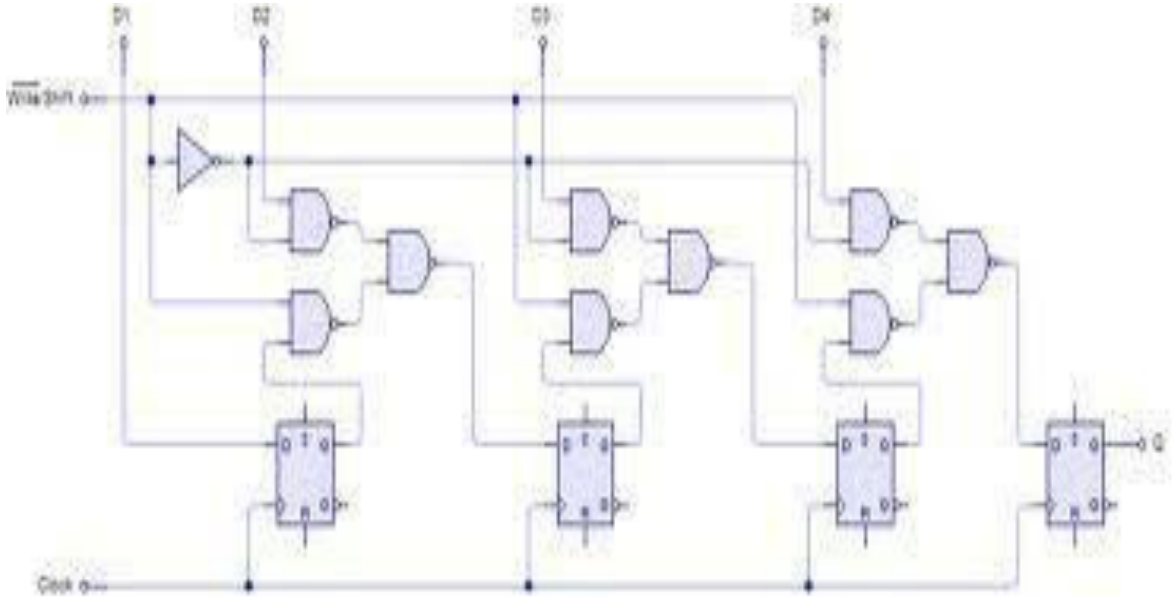


Serial-in, parallel-out, shift register:



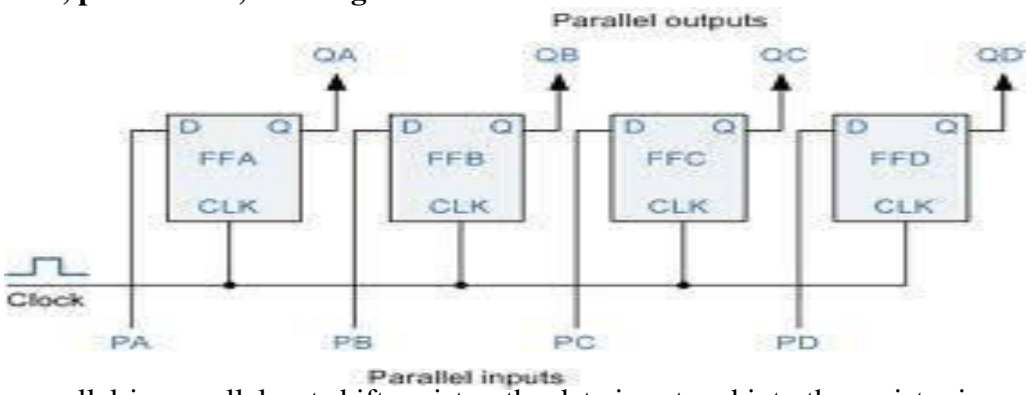
In this type of register, the data bits are entered into the register serially, but the data stored in the register is shifted out in parallel form.

Parallel-in, serial-out, shift register:



For a parallel-in, serial out, shift register, the data bits are entered simultaneously into their respective stages on parallel lines, rather than on a bit-by-bit basis on one line as with serial data bits are transferred out of the register serially. On a bit-by-bit basis over a single line.

Parallel-in, parallel-out, shift register



In a parallel-in, parallel-out shift register, the data is entered into the register in parallel form, and also the data is taken out of the register in parallel form. Data is applied to the D input terminals of the FF‘s. When a clock pulse is applied, at the positive going edge of the pulse, the D inputs are shifted into the Q outputs of the FFs. The register now stores the data. The stored data is available instantaneously for shifting out in parallel form.

Counters:

Counter is a device which stores (and sometimes displays) the number of times particular event or process has occurred, often in relationship to a clock signal. A Digital counter is a set of flip flops whose state change in response to pulses applied at the input to the counter. Counters may be asynchronous counters or synchronous counters. Asynchronous counters are also called ripple counters

In electronics counters can be implemented quite easily using register-type circuits such as the flip-flops and a wide variety of classifications exist:

- Asynchronous (ripple) counter – changing state bits are used as clocks to subsequent state flip-flops
- Synchronous counter – all state bits change under control of a single clock
- Decade counter – counts through ten states per stage
- Up/down counter – counts both up and down, under command of a control input
- Ring counter – formed by a shift register with feedback connection in a ring
- Johnson counter – a *twisted* ring counter
- Cascaded counter
- Modulus counter.

Occasionally there are advantages to using a counting sequence other than the natural binary sequence such as the binary coded decimal counter, a linear feed-back shift register counter, or a gray-code counter.
Counters are useful for digital clocks and timers, and in oven timers, VCR clocks, etc.