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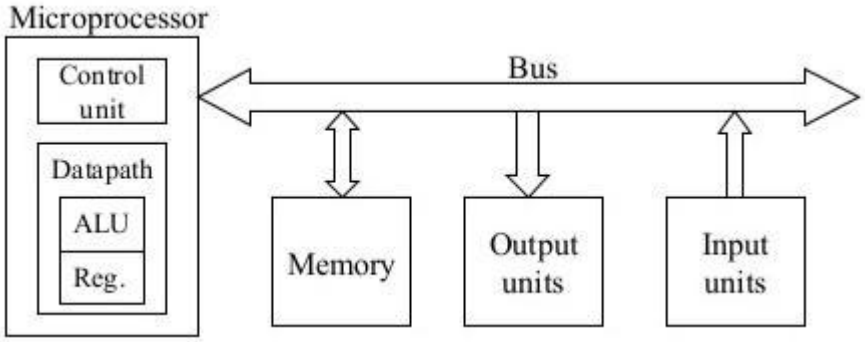
Department of Electronics and Communication Engineering

Bridge Course
On
Embedded Systems

Microprocessors-Evolution and Introduction:

- The microprocessor is an electronic chip that functions as the central processing unit of a computer.
- Microprocessor based systems with limited resources are called microcomputers.
- Today microprocessor found in almost all consumer electronic devices such as computer printers, washing machines, microwave ovens and in advanced applications such as satellites, radars and flights.

MICROPROCESSOR BASED SYSTEM:



A microprocessor-based system consists primarily of three components-the microprocessor unit (MPU), Memory and I/O (input / output). The MPU is the central player; it communicates with memory and I/O devices. Processes data, and controls timing of all its operations. Memory and 1I0s are integral parts of a microprocessor-based system.

The steps in performing these MPU operations can be summarized as follows (not necessarily in the order listed in every operation):

1. Identify the memory location or the peripheral with its address.
2. Provide timing or synchronization signal.
3. Transfer binary data

Therefore, the MPU requires three sets of communication lines called buses: the first group of lines, called the address bus, to identify the memory location; the second group, called the data bus, to transfer data; and the third group, called the control lines, for timing signals.

ADDRESS BUS:

If the address size is 4 bits, the microprocessor can identify 16 (24) different memory locations. The addressing is simply a numbering scheme to identify memory registers. For example, a two-digit decimal numbering scheme can identify only 100 items, from 00 to 99. On the other hand, a four-digit numbering scheme can identify 10,000 items, from 0000 to 9999. Thus, the number of bits (address Lines) used for addressing by the MPU clearly determines the number of memory registers it can identify. If there are n no of address line 2^n memory locations.

DATA BUS:

These lines are used to transfer data and are bidirectional-data can flow either direction. These lines are identified as D_0 to D_n where $_n$ signifies the most significant bit (MSB) of the data bus. Again, the size of the data bus determines how large a binary number can be transferred and processed at a time and thus influences the microprocessor architecture considerably

CONTROL BUS:

These are individual signal lines generated by the MPU to indicate its operations. The MPU generates a specific signal for each of its four operations-Memory Read. Memory Write, 1/0 Read, and I/O Write. These are timing signals that are used to enable, or activate, peripherals. For example, to fetch (or read) an instruction from a memory location, the MPU sends a timing pulse called Memory Read to enable the memory chip.

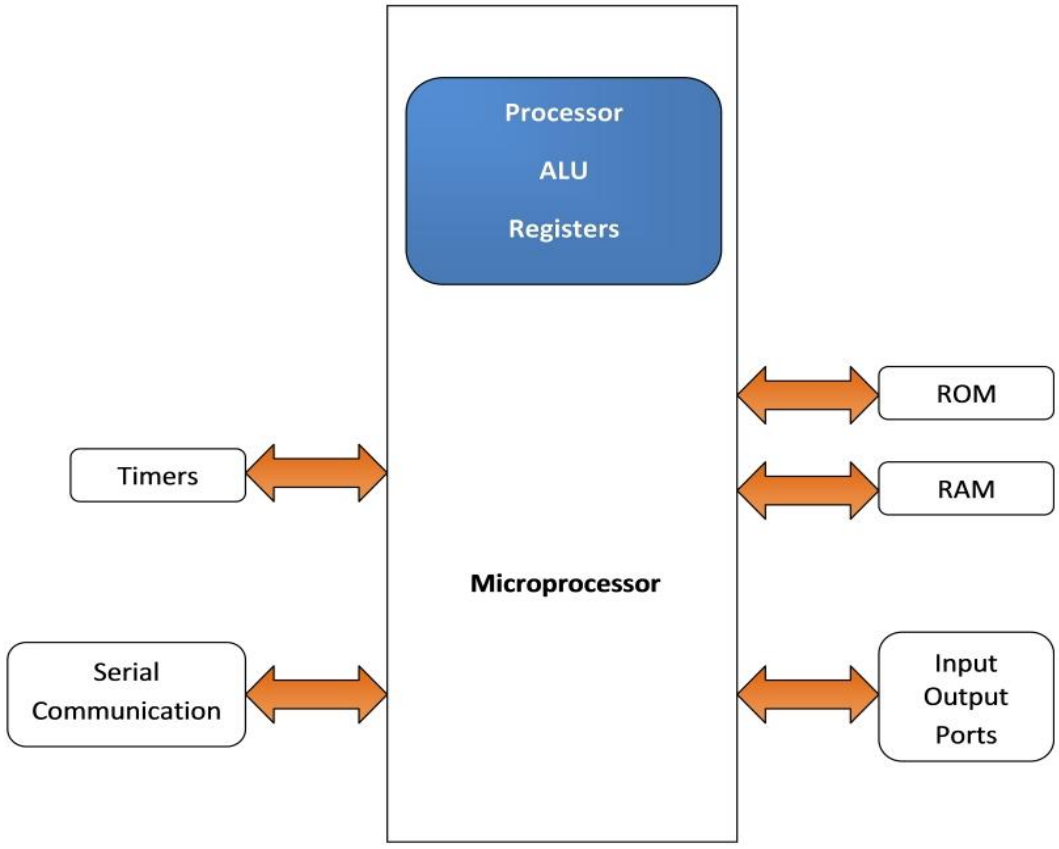


Fig: Microprocessor Basic block diagram

INTRODUCTION TO MICRO CONTROLLERS 8051:

To make a complete microcomputer system, only microprocessor is not sufficient. It is necessary to add other peripherals such as ROM, RAM, decoders, drivers, number of I/O devices to make a complete microcomputer system. In addition, special purpose devices, such as interrupt controller,

programmable timers, programmable I/O devices, DMA controllers may be added to improve the capability and performance and flexibility of a microcomputer system.

The key feature for microprocessor based design is that it has more flexibility to configure a system as large system or small system by adding suitable peripherals.

On the other hand, the microcontroller incorporates all the features that are found in microprocessor. The microcontroller has built-in ROM, RAM, parallel I/O, serial I/O, counters and a clock circuit. It has on-chip peripheral devices which makes it possible to have single microcomputer system.

Advantages of built-in peripherals:

- Built-in peripherals have smaller access times hence speed is more.
- Hardware reduces due to single chip microcomputer system.
- Less hardware reduces PCB size and increases reliability of the system.

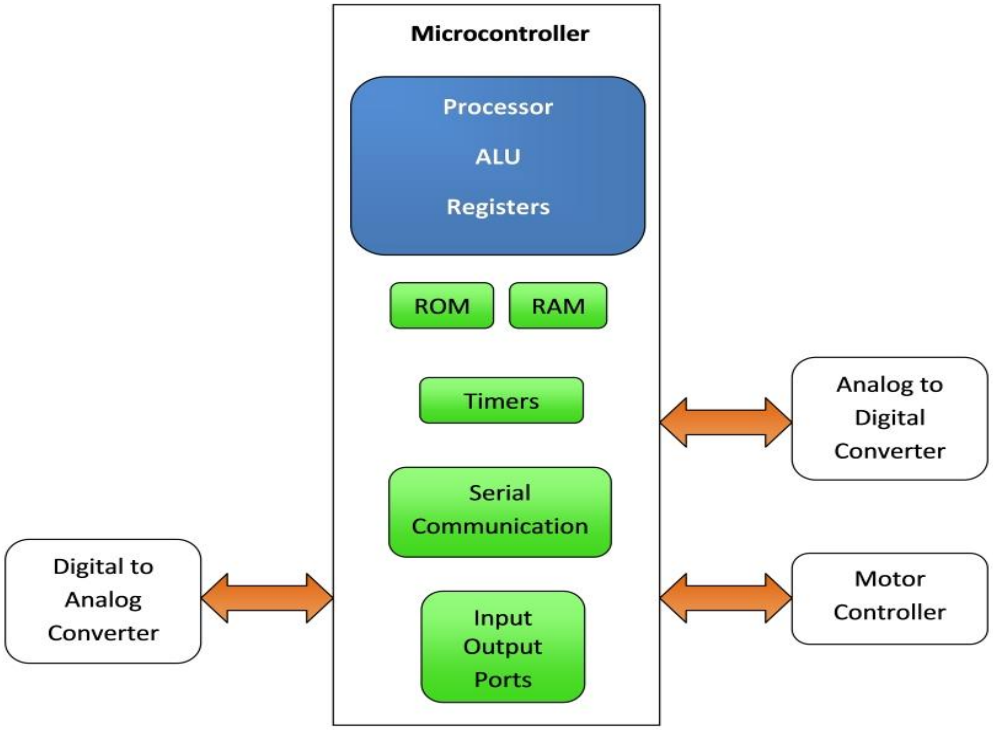


Fig: Microcontroller basic block diagram

Difference between Microprocessor and microcontroller:

1. Key difference in both of them is presence of external peripheral, where microcontrollers have RAM, ROM, EEPROM embedded in it while we have to use external circuits in case of microprocessors.
2. As all the peripheral of microcontroller are on single chip it is compact while microprocessor is bulky.

3. Microcontrollers are made by using complementary metal oxide semiconductor technology so they are far cheaper than microprocessors. In addition the applications made with microcontrollers are cheaper because they need lesser external components, while the overall cost of systems made with microprocessors are high because of the high number of external components required for such systems.

4. Processing speed of microcontrollers is about 8 MHz to 50 MHz, but in contrary processing speed of general microprocessors is above 1 GHz so it works much faster than microcontrollers.

5. Generally microcontrollers have power saving system, like idle mode or power saving mode so overall it uses less power and also since external components are low overall consumption of power is less. While in microprocessors generally there is no power saving system and also many external components are used with it, so its power consumption is high in comparison with microcontrollers.

6. Microcontrollers are compact so it makes them favorable and efficient system for small products and applications while microprocessors are bulky so they are preferred for larger applications.

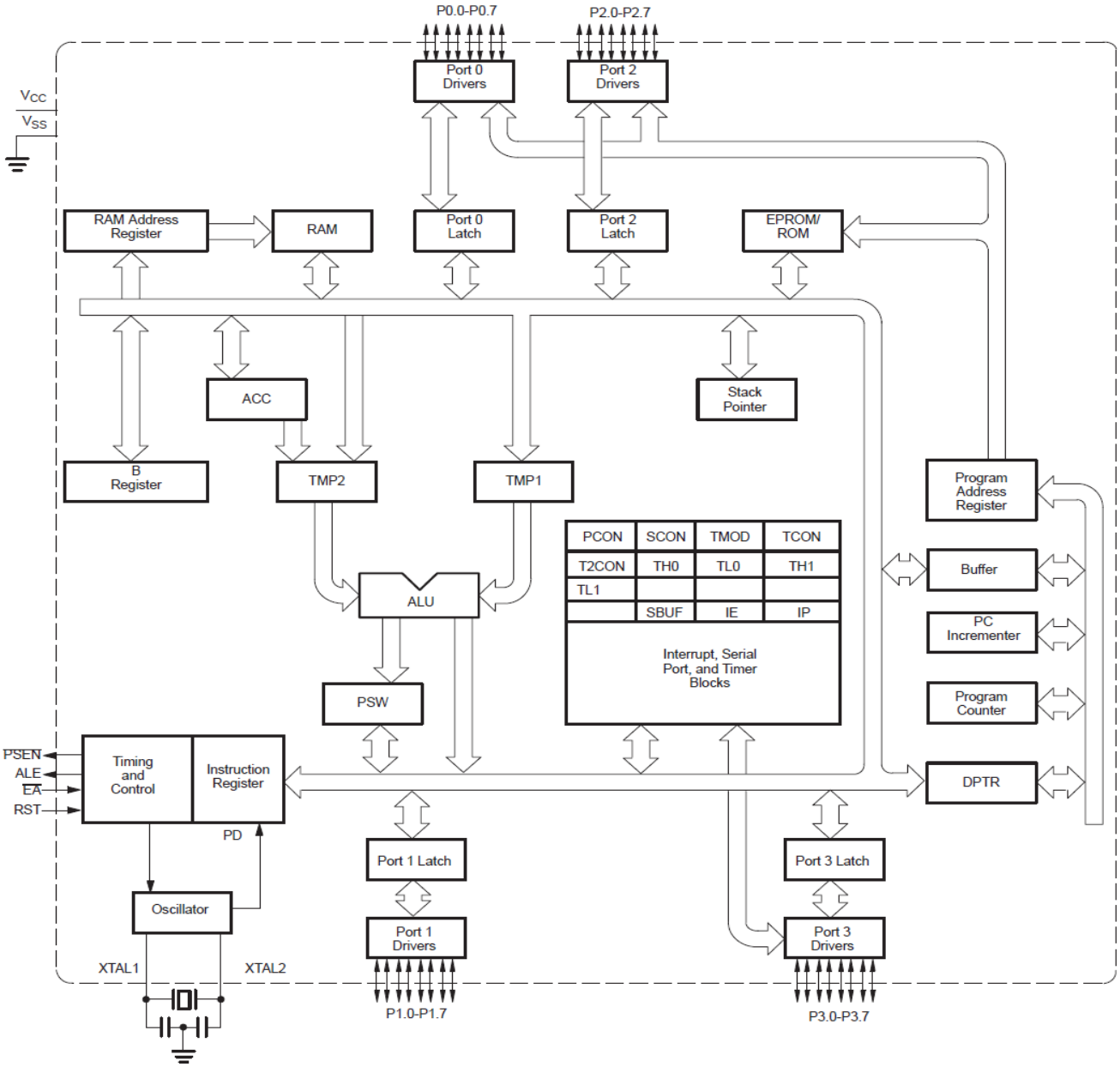
7. Tasks performed by microcontrollers are limited and generally less complex. While task performed by microprocessors are software development, Game development, website, documents making etc. which are generally more complex so require more memory and speed so that's why external ROM, RAM are used with it.

8. Microcontrollers are based on Harvard architecture where program memory and data memory are separate while microprocessors are based on von Neumann model where program and data are stored in same memory module.

Features of 8051:

- 4KB on-chip program memory (ROM/EPROM).
- 128 bytes on-chip data memory.
- Four register banks.
- 64KB each program and external RAM addressability.
- One microsecond instruction cycle with 12MHz crystal.
- 32 bidirectional I/O lines organized as four 8-bit ports.
- Multiple modes, high-speed programmable serial port (UART).
- 16-bit Timers/Counters.
- Direct byte and bit addressability.

Block Diagram of 8051:



Accumulator: The Accumulator, as it's name suggests, is used as a general register to accumulate the results of a large number of instructions. It can hold an 8-bit (1-byte) value.

'B' Register: The "B" register is very similar to the Accumulator in the sense that it may hold an 8-bit (1-byte) value. The "B" register is only used by two 8051 instructions: MUL AB and DIV AB.

Aside from the MUL and DIV an instruction, the "B" register is often used as yet another temporary storage register much like a ninth "R" register.

Program Status Word

The PSW register contains program status information. It is a 8-bit flag register, out of 8-bits 6 bits are used and 2 bits are reserved. Out of 6 bits 4 bits are conditional bits and 2 bits are used for selecting register bank.

MSB LSB

CY	AC	F0	RS1	RS0	OV	—	P

BIT	SYMBOL	FUNCTION
PSW.7	CY	Carry flag.
PSW.6	AC	Auxilliary Carry flag. (For BCD operations.)
PSW.5	F0	Flag 0. (Available to the user for general purposes.)
PSW.4	RS1	Register bank select control bit 1. Set/cleared by software to determine working register bank. (See Note.)
PSW.3	RS0	Register bank select control bit 0. Set/cleared by software todetermine working register bank. (See Note.)
PSW.2	OV	Overflow flag.
PSW.1	—	User-definable flag.
PSW.0	P	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the Accumulator, i.e., even parity.

NOTE: The contents of (RS1, RS0) enable the working register banks as follows:
(0,0)— Bank 0 (00H–07H)
(0,1)— Bank 1 (08H–0fH)
(1,0)— Bank 2 (10H–17H)
(1,1)— Bank 3 (18H–17H)

Stack Pointer

The Stack Pointer register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at locations 08H.

Data Pointer: The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

Program Counter

The Program Counter (PC) is a 2-byte address which tells the 8051 where the next instruction to execute is found in memory. When the 8051 is initialized PC always starts at 0000h and is incremented each time an instruction is executed. It is important to note that PC isn't always incremented by one. Since some instructions require 2 or 3 bytes the PC will be incremented by 2 or 3 in these cases.

The Program Counter is special in that there is no way to directly modify its value. That is to say, we can't do something like PC=2430h. On the other hand, if we execute LJMP 2430h you've effectively accomplished the same thing.

Ports 0 to 3

P0, P1, P2, and P3 are the SFR latches of Ports 0, 1, 2, and 3, respectively. Writing a one to a bit of a port SFR (P0, P1, P2, or P3) causes the corresponding port output pin to switch high. Writing a zero causes the port output pin to switch low. When used as an input, the external state of a port pin will be held in

the port SFR (i.e., if the external state of a pin is low, the corresponding port SFR bit will contain a 0; if it is high, the bit will contain a 1).

Serial Data Buffer

The Serial Buffer is actually two separate registers, a transmit buffer and a receive buffer. When data is moved to SBUF, it goes to the transmit buffer and is held for serial transmission. (Moving a byte to SBUF is what initiates the transmission.) When data is moved from SBUF, it comes from the receive buffer.

Timer Registers Basic to 80C51

Register pairs (TH0, TL0), and (TH1, TL1) are the 16-bit Counting registers for Timer/Counters 0 and 1, respectively.

Control Register for the 80C51

Special Function Registers IP, IE, TMOD, TCON, SCON, and PCON contain control and status bits for the interrupt system, the Timer/Counters, and the serial port.

Register Banks: The 8051 uses 8 "R" registers which are used in many of its instructions. These "R" registers are numbered from 0 through 7 (R0, R1, R2, R3, R4, R5, R6, and R7). These registers are generally used to assist in manipulating values and moving data from one memory location to another.

PSEN (Program Store Enable)

The8051 has four dedicated bus control signals. It is a control signal that enables external program (code) memory**.** It usually connects to an EPROM's Output Enable (OE) pin to permit reading of program bytes. The PSEN signal pulses low during the fetch stage of an instruction. When executing a program from internal ROM (8051/8052), PSEN remains in the inactive (high) state.

ALE (Address Latch Enable)

The 8051 similarly uses ALE for demultiplexing the address and data bus. When Port 0 is used in its alternate mode—as the data bus and the low-byte of the address bus—ALE is the signal that latches the address into an external register during the first half of a memory cycle.

EA (External Access)

The EA input signal is generally tied high (+5 V) or low (ground). If high, the 8051 executes programs from internal ROM when executing in the lower 4K of memory. If low, programs execute from external memory only (and PSEN pulses low accordingly).

RST (Reset)

The RST input is the master reset for the 8051. When this signal is brought high for at least two machine cycles, the 8051 internal registers are loaded with appropriate values for an orderly system start-up.

On-chip Oscillator Inputs

The 8051 features an on-chip oscillator. The nominal crystal frequency is 12 MHz for most ICs in the MCS-51™ family.

Memory Organization:

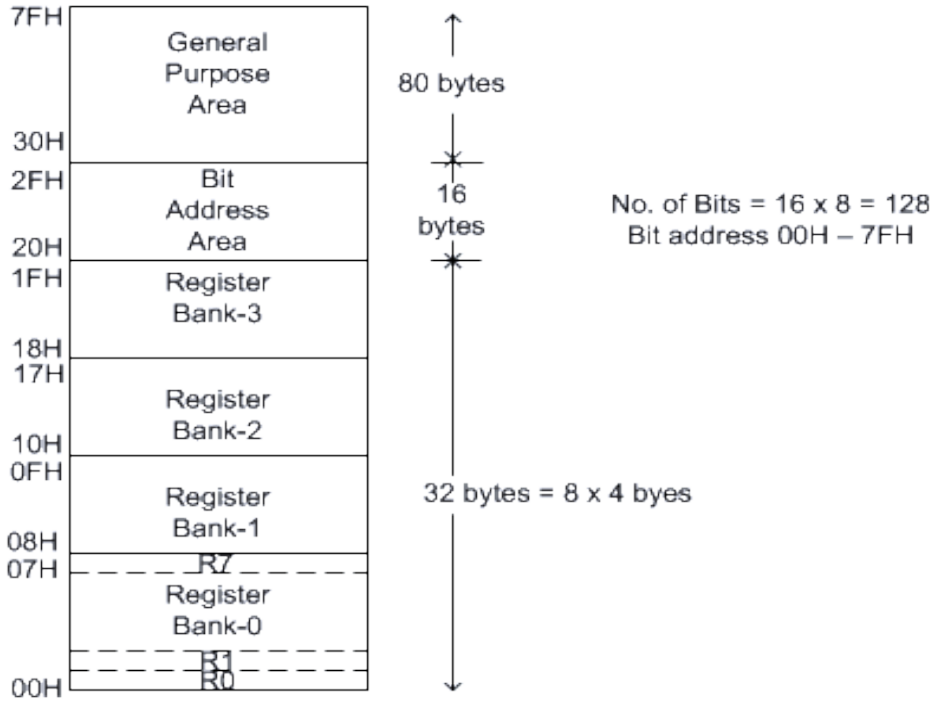
Most microprocessors implement a shared memory space for data and programs. This is reasonable, since programs are usually stored on a disk and loaded into RAM for execution; thus both

the data and programs reside in the system RAM. Microcontrollers have limited memory, andthere is no disk drive or disk operating system. The control program must reside in. For this reason, the 8051 implements a separate memory space for programs (code) and data. Both the code and data may be internal; however, both expand using external components to a maximum of 64K code memory and 64K data memory.

The internal memory consists of on-chip ROM (8051/8052 only) and on-chip data RAM. ***The on-chip RAM contains a rich arrangement of general-purpose storage, bit-addressable storage, register banks, and special function registers.***

The internal memory space is divided between register banks (00H-1FH), bit-addressable RAM (20H-2FH), general-purpose RAM (30H-7FH), and special function registers (80H-FFH). Any location in the general-purpose RAM can be accessed freely using the direct or indirect addressing modes.

Internal RAM memory:



Bit-addressable RAM

The 8051 contains 210 bit-addressable locations, of which 128 are at byte addresses 20H through 2FH, and the rest are in the special function registers.

The idea of individually accessing bits through software is a powerful feature of most microcontrollers. Bits can be set, cleared, ANDed, ORed, etc., with a single instruction.

Most microprocessors require a read-modify-write sequence of instructions to achieve the same effect. Furthermore, the 8051 I/O ports are bit-addressable, simplifying the software interface to single-bit inputs and outputs.

There are 128 general-purpose bit-addressable locations at byte address 20H through 2FH (8 bits/byte X 16 bytes = 128 bits).

Register Banks: The bottom 32 locations of internal memory contain the register banks. The 8051 instruction set supports 8 registers, R0 through R7, and by default (after a system reset) these registers are at addresses OOH-07H.

Instructions using registers R0 to R7 are shorter and faster than the equivalent instructions using direct addressing. Data values used frequently should use one of these registers.

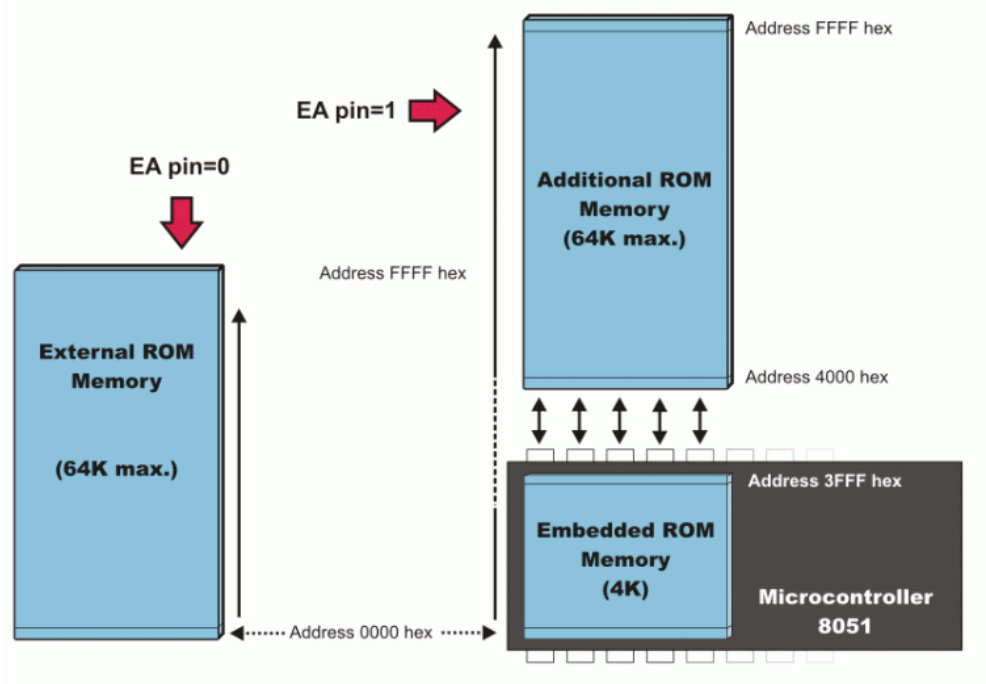
Special Function Registers

The 8051 internal registers are configured as part of the on-chip RAM; therefore, each register also has an address. This is reasonable for the 8051, since it has so many registers. As well as R0 to R7, there are 21 special function registers (SFRs) at the top of internal RAM, from addresses 80H to FFH.

EXTERNAL MEMORY

The MCS-51 architecture provides expansion in the form of a 64K external code memory space and a 64K external data memory space. Extra ROM and RAM can be added as needed. Peripheral interface ICs can also be added to expand the I/O capability. These *become* part of the external data memory space using memory-mapped I/O.

When external memory is used, Port 0 is unavailable as an I/O port. It becomes a multiplexed address (A0-A7) and data (D0-D7) bus, with ALE latching the low-byte of the address at the beginning of each external memory cycle. Port 2 is usually (but not always) employed for the high-byte of the address bus.



EA=0 In this case, the microcontroller completely ignores internal program memory and executes only the program stored in external memory.

EA=1 In this case, the microcontroller executes first the program from built-in ROM, then the program stored in external memory.

In both cases, P0 and P2 are not available for use since being used for data and address transmission. Besides, the ALE and PSEN pins are also used.

I/O Ports:

The four 8-bit I/O ports P0, P1, P2 and P3 each uses 8 pins. All the ports upon RESET are configured as output, ready to be used as input ports.

Port 0 is also designated as AD0-AD7, allowing it to be used for both address and data. When connecting an 8051/31 to an external memory, port 0 provides both address and data. The 8051 multiplexes address and data through port 0 to save pins.

ALE indicates if P0 has address or data.

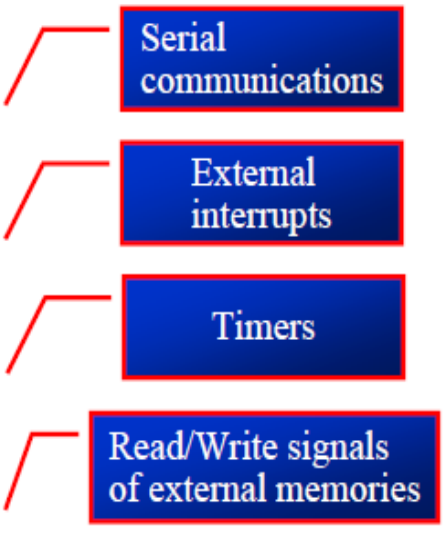
- When ALE=0, it provides data D0-D7
- When ALE=1, it has address A0-A7

In 8051-based systems with no external memory connection. Both P1 and P2 are used as simple I/O. In 8031/51-based systems with external memory connections, Port 2 must be used along with P0 to provide the 16-bit address for the external memory.

- P0 provides the lower 8 bits via A0 – A7
- P2 is used for the upper 8 bits of the 16-bit address, designated as A8 – A15, and it cannot be used for I/O Port 3 can be used as input or output.

Port 3 does not need any pull-up resistors. Port 3 has the additional function of providing some extremely important signals.

P3 Bit	Function	Pin
P3.0	RxD	10
P3.1	TxD	11
P3.2	$\overline{\text{INT0}}$	12
P3.3	$\overline{\text{INT1}}$	13
P3.4	T0	14
P3.5	T1	15
P3.6	$\overline{\text{WR}}$	16
P3.7	$\overline{\text{RD}}$	17



Counters and Timers:

Many microcontroller applications require the counting of external events, such as the frequency of a pulse train, or the generation of precise internal time delays between computer actions. To relieve the processor burden, two 16-bit upcounters, named T0 and T1, are provided for the general use of the programmer. Each counter may be programmed to count internal clock pulses, acting as a timer, or programmed to count external pulses as a counter. The timers are used for (a) interval timing, (b) event counting, or (c) baud rate generation for the built-in serial port.

The 8051 has two timers/counters, they can be used either as:

Timers to generate a time delay or as Event counters to count events happening outside the microcontroller

In interval timing applications, a timer is programmed to overflow at a regular interval and set the timer overflow flag. The flag is used to synchronize the program to perform an action such as checking the state of inputs or sending data to outputs.

Other applications can use the regular clocking of the timer to measure the elapsed time between two conditions (e.g., pulse width measurements).Event counting is used to determine the number of occurrences of an event, rather than to measure the elapsed time between events. An "event" is any external stimulus that provides a 1-to-0 transition to a pin on the 8051 IC. The timers can also provide the baud rate clock for the 8051's internal serial port.

SERIAL PORT OPERATION:

The 8051 includes an on-chip serial port that can operate in several modes over a wide range of frequencies. The essential function of the serial port is to perform parallel-to-serial conversion for output data, and serial-to-parallel conversion for input data.

The serial port features **Full duplex** operation (simultaneous transmission and reception), and **receive buffering allowing** one character to be received and held in a buffer while a second character is received. If the CPU reads the first character before the second is fully received, data are not lost.

Two special function registers provide software access to the serial port, SBUF and SCON. The serial port buffer (SBUF) at address 99H is really two buffers. Writing to SBUF loads data to be transmitted, and reading SBUF accesses received data. These are two separate and distinct registers, the transmit write-only register, and the receive read-only register.