G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) SET-1

IV B.Tech.I SEM, II MID Objective Exam Branch: ECE

Sub: VLSI DESIGN **Date : 7-11-17**

Time: 20 min **Max.Marks:10**

Roll No: **Invigilator signature:**

==========

1. Tool used to generate netlist ( )
a. simulator b. compiler c. synthesizer d. assembler

2. Method of computing the expected timing of signals inside a digital circuit without simulation. ( )
a. STA b .clock tree synthesis c. simulation d. netlist

3. Conditional sum adder is also called as ( )
a. carry skip b. carry look ahead c. carry select d. ripple carry

4. A digital processor consists of ( )
a. Datapath b.memory c.control d.all

5. Most commonly used logic blocks in FPGA ( )
a. multipliers b. adders c. LUTs d. multiplexers

6. Heart of ALU is ( )
a. adder b. mux c. comparator d. counter

7.Physical imperfection that may lead to a fault ( )
a. perfect b. defect c. yield d. demux

8.Testing the circuit with all possible input patterns. ( )
a. Exhaustive b. Adhoc c. BIST d. signature analysis

9. Fastest multiplier ( )
a. serial parallel b. modified booth c. braun array d. baugh wooley

10. Delay of clock appearing at various functional units is called as ( )
a. clock skew b.critical path c.clock routing d. CTS

11.Modularity ensures that sub modules have well defined functions and interfaces. [T/F]

12.Test bench simulates the module under test and observes its behavior. [T/F]

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11.Modularity ensures that sub modules have well defined functions and interfaces. [T/F]

12.Test bench simulates the module under test and observes its behavior. [T/F]

13.DRAM is used in cache memory. [T/F]

14.LSSD stands for Level Sensitive Standard Design. [T/F]

15.Single phase dynamic structures cannot be cascaded. [T/F]

16.Logic optimization aims at _____silicon area.

17._____allows the description of the structure of a hardware system.

18.DRAM has to be _____ to retain the logic value.

19.The process of removing intermediate signals to produce an optimized design is_____

20. Simulating a circuit in the presence of faults is called as _____

13.DRAM is used in cache memory. [T/F]

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G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) SET-2

IV B.Tech.I SEM, II MID Objective Exam Branch: ECE

Sub: VLSI DESIGN **Date : 7-11-17**

Time: 20 min **Max.Marks:10**

Roll No: **Invigilator signature:**

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1. Logic optimization aims at _____silicon area.

2. _____allows the description of the structure of a hardware system.

3. DRAM has to be _____ to retain the logic value.

4. The process of removing intermediate signals to produce an optimized design is_____

5. Simulating a circuit in the presence of faults is called as _____

6. Heart of ALU is ( )
a. adder b. mux c. comparator d. counter

7. Physical imperfection that may lead to a fault ( )
a. perfect b. defect c. yield d. demux

8. Testing the circuit with all possible input patterns. ( )
a. Exhaustive b. Adhoc c. BIST d. signature analysis

9. Fastest multiplier ( )
a. serial parallel b. modified booth c. braun array d. baugh wooley

10. Delay of clock appearing at various functional units is called as ( )
a. clock skew b.critical path c.clock routing d. CTS

11. Tool used to generate netlist ( )
a. simulator b. compiler c. synthesizer d. assembler

12. Method of computing the expected timing of signals inside a digital circuit without simulation. ( )
a. STA b .clock tree synthesis c. simulation d. netlist

G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) SET-2

IV B.Tech.I SEM, II MID Objective Exam Branch: ECE

Sub: VLSI DESIGN **Date : 7-11-17**

Time: 20 min **Max.Marks:10**

Roll No: **Invigilator signature:**

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1. Logic optimization aims at _____silicon area.

2. _____allows the description of the structure of a hardware system.

3. DRAM has to be _____ to retain the logic value.

4. The process of removing intermediate signals to produce an optimized design is_____

5. Simulating a circuit in the presence of faults is called as _____

6. Heart of ALU is ( )
a. adder b. mux c. comparator d. counter

7. Physical imperfection that may lead to a fault ( )
a. perfect b. defect c. yield d. demux

8. Testing the circuit with all possible input patterns. ( )
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12. Method of computing the expected timing of signals inside a digital circuit without simulation. ( )
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G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) SET-3

IV B.Tech.I SEM, II MID Objective Exam Branch: ECE

Sub: VLSI DESIGN **Date : 7-11-17**

Time: 20 min **Max.Marks:10**

Roll No: **Invigilator signature:**

==========

1.Modularity ensures that sub modules have well defined functions and interfaces. [T/F]

2.Test bench simulates the module under test and observes its behavior. [T/F]

3.DRAM is used in cache memory. [T/F]

4.LSSD stands for Level Sensitive Standard Design. [T/F]

5.Single phase dynamic structures cannot be cascaded. [T/F]

6.Logic optimization aims at _____silicon area.

7. _____allows the description of the structure of a hardware system.

8. DRAM has to be _____ to retain the logic value.

9. The process of removing intermediate signals to produce an optimized design is_____

10. Simulating a circuit in the presence of faults is called as _____

11. Heart of ALU is ( )
a. adder b. mux c. comparator d. counter

12. Physical imperfection that may lead to a fault ( )
a. perfect b. defect c. yield d. demux

13. Testing the circuit with all possible input patterns. ( )
a. Exhaustive b. Adhoc c. BIST d. signature analysis

14. Fastest multiplier ( )
a. serial parallel b. modified booth c. braun array d. baugh wooley

15. Delay of clock appearing at various functional units is called as ( )
a. clock skew b.critical path c.clock routing d. CTS

G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) SET-3

IV B.Tech.I SEM, II MID Objective Exam Branch: ECE

Sub: VLSI DESIGN **Date : 7-11-17**

Time: 20 min **Max.Marks:10**

Roll No: **Invigilator signature:**

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1.Modularity ensures that sub modules have well defined functions and interfaces. [T/F]

2.Test bench simulates the module under test and observes its behavior. [T/F]

3.DRAM is used in cache memory. [T/F]

4.LSSD stands for Level Sensitive Standard Design. [T/F]

5.Single phase dynamic structures cannot be cascaded. [T/F]

6.Logic optimization aims at _____silicon area.

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16. Tool used to generate netlist ( )
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18. Conditional sum adder is also called as ( )
a. carry skip b. carry look ahead c. carry select d. ripple carry

19. A digital processor consists of ( )
f. datapath b. memory c. control d. all

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G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) SET-4

IV B.Tech.I SEM, II MID Objective Exam Branch: ECE

Sub: VLSI DESIGN **Date : 7-11-17**

Time: 20 min **Max.Marks:10**

Roll No: **Invigilator signature:**

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c. STA b .clock tree synthesis c. simulation d. netlist

3. Conditional sum adder is also called as ( )
a. carry skip b. carry look ahead c. carry select d. ripple carry

4. A digital processor consists of ( )
g. Datapath b.memory c.control d.all

5. Most commonly used logic blocks in FPGA ( )
a. multipliers b. adders c. LUTs d. multiplexers

6. Heart of ALU is ( )
a. adder b. mux c. comparator d. counter

7.Physical imperfection that may lead to a fault ( )
a. perfect b. defect c. yield d. demux

8.Testing the circuit with all possible input patterns. ( )
a. Exhaustive b. Adhoc c. BIST d. signature analysis

9. Fastest multiplier ( )
a. serial parallel b. modified booth c. braun array d. baugh wooley

10. Delay of clock appearing at various functional units is called as ( )
a. clock skew b.critical path c.clock routing d. CTS

G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) SET-4

IV B.Tech.I SEM, II MID Objective Exam Branch: ECE

Sub: VLSI DESIGN **Date : 7-11-17**

Time: 20 min **Max.Marks:10**

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d. STA b .clock tree synthesis c. simulation d. netlist

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4. A digital processor consists of ( )
h. Datapath b.memory c.control d.all

5. Most commonly used logic blocks in FPGA ( )
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6. Heart of ALU is ( )
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11. Logic optimization aims at _____silicon area.

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14. The process of removing intermediate signals to produce an optimized design is_____

15. Simulating a circuit in the presence of faults is called as _____

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