G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY

III B.Tech. II Sem., I MID Objective Exam

Branch: ECE & EEE

SET-1

SUB: MPMC **Date: 28-02-2018**

TIME: 20Min **Max Marks: 10M**

Hall Ticket No: | | | | | | | | | | | **Signature of Invigilator:**

I - Choose the correct answer:

1) What is the length of instruction Queue in 8086 _____ [ ]
(A) 4 bytes (B) 6 bytes (C) 5 bytes (D) None

2) Memory capacity of 8086 microprocessor [ ]
(A) 512 KB (B) 2 MB (C) 64 KB (D) None

3) The index registers are used to hold _____ address [ ]
(A) Offset (B) Segment (C) physical (D) None

4) _____ pin separates the multiplexed address and data lines in 8086 [ ]
(A) BHE' (B) MN/MX' (C) ALE (D) None

5) _____ is a breakpoint interrupt in 8086 [ ]
(A) Type 0 (B) Type 3 (C) Type 2 (D) None

6) 8086 operates in _____ modes. [ ]
(A) 1 (B) 3 (C) 2 (D) All

7) _____ Flag is set when the carry forwarded from lower nibble to upper nibble(D3 to D4) [ ]
(A)Carry (B) Auxiliary carry (C) Parity (D) None

8) What is the size of offset address in 8086 [ ]
(A) 16-bit (B) 20-bit (C) 18-bit (D) None

9) What is the address bus size of 8086 [ ]
(A) 16-bit (B) 20-bit (C) 8-bit (D) None

10) How many interrupts are there in 8086_____ [ ]
(A) 256 (B) 00-FF h (C) Both A & B (D) None

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11) The instruction, MOV AX, 0005H belongs to the address mode [ ]
(A) Direct (B) Indirect (C) Immediate (D) None
12) If the offset of the operand is stored in one of the index registers, then it is [ ]
(A) Indirect (B) Indexed (C) Immediate (D) None
13) In PUSH instruction, after each execution of the instruction, the stack pointer is [ ]
(A) Incremented by 1 (B) Decremented by 1 (C) Decremented by 2 (D) None
14) During comparison operation, the result of comparing or subtraction is stored [ ]
(A) Memory (B) Stack (C) Registers (D) No where
15) The ROR instruction rotates the contents of the destination operand to [ ]
(A) Left (B) Right (C) Right with Carry (D) None
16) The directive that marks the end of a logical segment is [ ]
(A) ENDS (B) ENDP (C) END (D) None
17) The instruction that is not possible among the following is [ ]
(A) MOV AX, BX (B) MOV AX, [BX] (C) MOV 55H, AL (D) None
18) The instruction that loads the AH register with the lower byte of the flag register is [ ]
(A)LAHF (B) SAHF (C) POPF (D) None
19) The instruction is used for finding out the codes in case of code conversion problems is [ ]
(A) XCHG (B) XLAT (C) JCXZ (D) None
20) The extension that is essential for every assembly level program is [ ]
(A) .ALP (B) .ASM (C) .ASP ASP (D) None

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G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY
III B.Tech. II Sem., I MID Objective Exam
Branch: ECE & EEE

SET-2

SUB: MPMC **Date: 28-02-2018**
TIME: 20Min **Max Marks: 10M**
Hall Ticket No: | | | | | | | | | | | **Signature of Invigilator:**

I - Choose the correct answer:

1) _____ pin separates the multiplexed address and data lines in 8086 [ ]
(A) BHE' (B) MN/MX' (C) ALE (D) None

2) _____ is a breakpoint interrupt in 8086 [ ]
(A) Type 0 (B) Type 3 (C) Type 2 (D) None

3) 8086 operates in _____ modes. [ ]
(A) 1 (B) 3 (C) 2 (D) All

4) What is the address bus size of 8086 [ ]
(A) 16-bit (B) 20-bit (C) 8-bit (D) None

5) How many interrupts are there in 8086_____ [ ]
(A) 256 (B) 00-FF h (C) Both A & B (D) None

6) Memory capacity of 8086 microprocessor [ ]
(A) 512 KB (B) 2 MB (C) 64 KB (D) None

7) The index registers are used to hold _____ address [ ]
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8) _____ Flag is set when the carry forwarded from lower nibble to upper nibble(D3 to D4) [ ]
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9) What is the size of offset address in 8086 [ ]
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10) What is the length of instruction Queue in 8086 _____ [ ]
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III B.Tech. II Sem., I MID Objective Exam
Branch: ECE & EEE

SET-2

SUB: MPMC Date: 28-02-2018
TIME: 20Min Max Marks: 10M
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11) In PUSH instruction, after each execution of the instruction, the stack pointer is [ ]
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12) During comparison operation, the result of comparing or subtraction is stored [ ]
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13) The instruction that loads the AH register with the lower byte of the flag register is [ ]
(A)LAHF (B) SAHF (C) POPF (D) None
14) The instruction is used for finding out the codes in case of code conversion problems is [ ]
(A) XCHG (B) XLAT (C) JCXZ (D) None
15) The instruction, MOV AX, 0005H belongs to the address mode [ ]
(A) Direct (B) Indirect (C) Immediate (D) None
16) If the offset of the operand is stored in one of the index registers, then it is [ ]
(A) Indirect (B) Indexed (C) Immediate (D) None
17) The instruction that is not possible among the following is [ ]
(A) MOV AX, BX (B) MOV AX, [BX] (C) MOV 55H, AL (D) None
18) The extension that is essential for every assembly level program is [ ]
(A) .ALP (B) .ASM (C) .ASP (D) None
19) The directive that marks the end of a logical segment is [ ]
(A) ENDS (B) ENDP (C) END (D) None
20) The ROR instruction rotates the contents of the destination operand to [ ]
(A) Left (B) Right (C) Right with Carry (D) None

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III B.Tech. II Sem., I MID Objective Exam
Branch: ECE & EEE

SET-3

SUB: MPMC **Date: 28-02-2018**
TIME: 20Min **Max Marks: 10M**
Hall Ticket No: | | | | | | | | | | | **Signature of Invigilator:**

I - Choose the correct answer:

1) 8086 operates in _____ modes. [ ]
(A) 1 (B) 3 (C) 2 (D) All

2) What is the address bus size of 8086 [ ]
(A) 16-bit (B) 20-bit (C) 8-bit (D) None

3) What is the size of offset address in 8086 [ ]
(A) 16-bit (B) 20-bit (C) 18-bit (D) None

4) What is the length of instruction Queue in 8086 _____ [ ]
(A) 4 bytes (B) 6 bytes (C) 5 bytes (D) None

5) How many interrupts are there in 8086_____ [ ]
(A) 256 (B) 00-FF h (C) Both A & B (D) None

6) Memory capacity of 8086 microprocessor [ ]
(A) 512 KB (B) 2 MB (C) 64 KB (D) None

7) _____ pin separates the multiplexed address and data lines in 8086 [ ]
(A) BHE' (B) MN/MX' (C) ALE (D) None

8) _____ is a breakpoint interrupt in 8086 [ ]
(A) Type 0 (B) Type 3 (C) Type 2 (D) None

9) The index registers are used to hold _____ address [ ]
(A) Offset (B) Segment (C) physical (D) None

10) _____ Flag is set when the carry forwarded from lower nibble to upper nibble(D3 to D4) [ ]
(A)Carry (B) Auxiliary carry (C) Parity (D) None

G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY
III B.Tech. II Sem., I MID Objective Exam
Branch: ECE & EEE

SUB: MPMC **Date: 28-02-2018**
TIME: 20Min **Max Marks: 10M**
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I - Choose the correct answer:

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2) What is the address bus size of 8086 [ ]
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III B.Tech. II Sem., I MID Objective Exam

Branch: ECE & EEE

SET-4

SUB: MPMC **Date: 28-02-2018**

TIME: 20Min **Max Marks: 10M**

Hall Ticket No: | | | | | | | | | | | **Signature of Invigilator:**

I - Choose the correct answer:

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5) _____ pin separates the multiplexed address and data lines in 8086 [ ]
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7) 8086 operates in _____ modes. [ ]
(A) 1 (B) 3 (C) 2 (D) All

8) What is the address bus size of 8086 [ ]
(A) 16-bit (B) 20-bit (C) 8-bit (D) None

9) Memory capacity of 8086 microprocessor [ ]
(A) 512 KB (B) 2 MB (C) 64 KB (D) None

10) What is the size of offset address in 8086 [ ]
(A) 16-bit (B) 20-bit (C) 18-bit (D) None

G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY

III B.Tech. II Sem., I MID Objective Exam

Branch: ECE & EEE

SET-4

SUB: MPMC **Date: 28-02-2018**

TIME: 20Min **Max Marks: 10M**

Hall Ticket No: | | | | | | | | | | | **Signature of Invigilator:**

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