

9) What is the address bus size of 8086

10) How many interrupts are there in 8086\_

(B) 20-bit

(B) 00-FF h

(A) 16-bit

(A) 256

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SET-1

[

(D) None

(D) None

]

]

### III B.Tech. II Sem., I MID Objective Exam

**Branch: ECE & EEE** 

SUB: MPMC TIME: 20Min Hall Ticket No:	Date: 28-02-2018  Max Marks: 10M  Signature of Invigilator
I - Choose the correct answer:	
1) What is the length of instruction Queue in 8086	
	bytes (D) None
2) Memory capacity of 8086 microprocessor	54 KB (D) None
	` '
3) The index registers are used to hold address (A) Offset (B) Segment (C) p	ess [Dhysical (D) None
4) pin separates the multiplexed address and d	· ·
(A) BHE' (B) MN/MX' (C) A	
5) is a breakpoint interrupt in 8086	[
	Type 2 (D) None
6) 8086 operates in modes.	
(A) 1 (B) 3 (C) 2	(D) All
7) Flag is set when the carry forwarded from	11
	Parity (D) None
8) What is the size of offset address in 8086	
	8-bit (D) None
9) What is the address bus size of 8086 (A) 16-bit (B) 20-bit (C) 8	) hit (D) None
10) How many interrupts are there in 8086	B-bit (D) None
	Both A & B (D) None
GPCET III B.Tech. II Sem.,	I MID Objective Exam SET-1
	ECE & EEE
SUB:MPMC	Date: 28-02-2018
TIME: 20Min	Max Marks: 10M
Hall Ticket No:	Signature of Invigilator:
I - Choose the correct answer:	
1) What is the length of instruction Queue in 8086	
	bytes (D) None
2) Memory capacity of 8086 microprocessor	(D) N
	54 KB (D) None
3) The index registers are used to hold addres	-
4) pin separates the multiplexed address and d (A) BHE' (B) MN/MX' (C) A	
	ALE (D) None
is a breakpoint interrupt in 8086 (C) Type 0 (B) Type 3 (C) T	Гуре 2 (D) None
6) 8086 operates in modes.	Type 2 (D) None
(A) 1 (B) 3 (C) 2	(D) All
7) Flag is set when the carry forwarded from	
	Parity (D) None
8) What is the size of offset address in 8086	[
(A) 16-bit (B) 20-bit (C) 1	8-bit (D) None

(C) 8-bit

(C) Both A & B

11) The instruction, MOV AX, 0005H belongs to the address mode	[	]
(A) Direct (B) Indirect (C) Immediate (D) None		
12) If the offset of the operand is stored in one of the index registers, then it is	[	]
(A) Indirect (B) Indexed (C) Immediate (D) None		
13) In PUSH instruction, after each execution of the instruction, the stack pointer is	[	]
(A) Incremented by 1 (B) Decremented by 1 (C) Decremented by 2 (D) None		
14) During comparison operation, the result of comparing or subtraction is stored	[	]
(A) Memory (B) Stack (C) Registers (D) No where		
15) The ROR instruction rotates the contents of the destination operand to	[	]
(A) Left (B) Right (C) Right with Carry (D) None	-	-
16) The directive that marks the end of a logical segment is	[	]
(A) ENDS (B) ENDP (C) END (D) None		-
17) The instruction that is not possible among the following is	[	]
(A) MOV AX, BX (B) MOV AX, [BX] (C) MOV 55H, AL (D) None	L	,
18) The instruction that loads the AH register with the lower byte of the flag register is	[	]
(A)LAHF (B) SAHF (C) POPF (D) None	L	,
19) The instruction is used for finding out the codes in case of code conversion problems is	Γ	]
(A) XCHG (B) XLAT (C) JCXZ (D) None	L	,
20) The extension that is essential for every assembly level program is	[	]
(A) .ALP (B) .ASM (C) .ASP ASP (D) None	L	1
(1) .1L1 (D) .1DW (C) .1DI 11DI (D) 11OIC		
11) The instruction MOV AV 0005H belongs to the address made	ſ	1
11) The instruction, MOV AX, 0005H belongs to the address mode  (A) Direct  (B) Indirect  (C) Immediate  (D) None	[	]
(A) Direct (B) Indirect (C) Immediate (D) None	[	]
(A) Direct (B) Indirect (C) Immediate (D) None 12) If the offset of the operand is stored in one of the index registers, then it is	]	]
(A) Direct (B) Indirect (C) Immediate (D) None  12) If the offset of the operand is stored in one of the index registers, then it is  (A) Indirect (B) Indexed (C) Immediate (D) None	[	]
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<ul> <li>(A) Direct</li> <li>(B) Indirect</li> <li>(C) Immediate</li> <li>(D) None</li> <li>12) If the offset of the operand is stored in one of the index registers, then it is</li> <li>(A) Indirect</li> <li>(B) Indexed</li> <li>(C) Immediate</li> <li>(D) None</li> <li>13) In PUSH instruction, after each execution of the instruction, the stack pointer is</li> <li>(A) Incremented by 1</li> <li>(B) Decremented by 1</li> <li>(C) Decremented by 2</li> <li>(D) None</li> <li>14) During comparison operation, the result of comparing or subtraction is stored</li> </ul>	[	]
(A) Direct (B) Indirect (C) Immediate (D) None  12) If the offset of the operand is stored in one of the index registers, then it is (A) Indirect (B) Indexed (C) Immediate (D) None  13) In PUSH instruction, after each execution of the instruction, the stack pointer is (A) Incremented by 1 (B) Decremented by 1 (C) Decremented by 2 (D) None  14) During comparison operation, the result of comparing or subtraction is stored (A) Memory (B) Stack (C) Registers (D) No where	[	]
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(C) .ASP

(D) None

(A) .ALP

(B) .ASM



**SUB: MPMC** 

# $\underline{\textbf{G.PULLAIAH COLLEGE OF ENGINEERING \& TECHNOLOGY}}$

SET-2

Date: 28-02-2018

## III B.Tech. II Sem., I MID Objective Exam

**Branch: ECE & EEE** 

TIME: 20Min Hall Ticket No:		Max Marks: 10M Signature of Invigilator:	
I - Choose the correct answer:			
1) pin separates the multiplexed address a		[ D) None	]
		D) None	1
2) is a breakpoint interrupt in 808 (A) Type 0 (B) Type 3		D) None	J
	(C) Type 2 (1	) None	1
3) 8086 operates in modes. (A) 1 (B) 3	(C) 2	D) All	J
4) What is the address bus size of 8086	(C) 2	D) All	1
	(C) 8-bit (I	D) None	J
5) How many interrupts are there in 8086	_	[	1
	(C) Both A & B (1	D) None	-
6) Memory capacity of 8086 microprocessor		[	]
(A) $512 \text{ KB}$ (B) $2 \text{ MB}$	$(C) 64 KB \qquad (I)$	D) None	
7) The index registers are used to holda	address	[	]
(A) Offset (B) Segment	(C) physical (	(D) None	
8) Flag is set when the carry forwarded	d from lower nibble to uppe	er nibble(D3 to D4) [	]
(A)Carry (B) Auxiliary carry	(C) Parity (1	D) None	
9) What is the size of offset address in 8086		[	]
` '		D) None	
10) What is the length of instruction Queue in 8086	· ·	[	]
(A) 4 bytes (B) 6 bytes	(C) 5 bytes (1	D) None	
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	Sem., I MID Objective Exam	$\underline{\mathbf{m}}$   SET-2	
Pioneering Innovative Education Brain	nch: ECE & EEE		
Pronecting Innovative Education  SUB: MPMC		Date: 28-02-2018	
Proncering Innovative Education  SUB: MPMC  TIME: 20Min		Date: 28-02-2018 Max Marks: 10M	
Pronecting Innovative Education  SUB: MPMC		Date: 28-02-2018	·:
SUB: MPMC TIME: 20Min Hall Ticket No:		Date: 28-02-2018 Max Marks: 10M	
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the correct answer:	nch: ECE & EEE	Date: 28-02-2018  Max Marks: 10M  Signature of Invigilator	
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the correct answer:  1) pin separates the multiplexed address a	nch: ECE & EEE  nd data lines in 8086	Date: 28-02-2018  Max Marks: 10M  Signature of Invigilator	·: ::
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the correct answer:  1) pin separates the multiplexed address a (A) BHE' (B) MN/MX'	nch: ECE & EEE  and data lines in 8086 (C) ALE (1)	Date: 28-02-2018  Max Marks: 10M  Signature of Invigilator	·: ]
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the correct answer:  1) pin separates the multiplexed address a (A) BHE' (B) MN/MX'  2) is a breakpoint interrupt in 808	nch: ECE & EEE  nd data lines in 8086 (C) ALE (186	Date: 28-02-2018  Max Marks: 10M  Signature of Invigilator  [ D) None	.; ]
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the correct answer:  1) pin separates the multiplexed address a (A) BHE' (B) MN/MX'  2) is a breakpoint interrupt in 808 (A) Type 0 (B) Type 3	nch: ECE & EEE  nd data lines in 8086 (C) ALE (186	Date: 28-02-2018  Max Marks: 10M  Signature of Invigilator	": ]
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the correct answer:  1) pin separates the multiplexed address a (A) BHE' (B) MN/MX'  2) is a breakpoint interrupt in 808 (A) Type 0 (B) Type 3  3) 8086 operates in modes.	nch: ECE & EEE  and data lines in 8086 (C) ALE (C) Type 2 (1)	Date: 28-02-2018  Max Marks: 10M  Signature of Invigilator  [ D) None  [ D) None  [	": ] ]
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the correct answer:  1) pin separates the multiplexed address a (A) BHE' (B) MN/MX'  2) is a breakpoint interrupt in 808 (A) Type 0 (B) Type 3  3) 8086 operates in modes. (A) 1 (B) 3	nd data lines in 8086 (C) ALE (1866) (C) Type 2 (1869)	Date: 28-02-2018  Max Marks: 10M  Signature of Invigilator  [ D) None	": ] ]
SUB: MPMC   TIME: 20Min   Hall Ticket No:	nch: ECE & EEE  nd data lines in 8086 (C) ALE (1866) (C) Type 2 (1876) (C) 2 (1876)	Date: 28-02-2018  Max Marks: 10M  Signature of Invigilator  [ D) None  [ D) None  [ D) All  [	]
SUB: MPMC   TIME: 20Min   Hall Ticket No:	nch: ECE & EEE  nd data lines in 8086 (C) ALE (1866) (C) Type 2 (1876) (C) 2 (1876)	Date: 28-02-2018  Max Marks: 10M  Signature of Invigilator  [ D) None  [ D) None  [	": ] ]
SUB: MPMC   TIME: 20Min   Hall Ticket No:	nch: ECE & EEE  and data lines in 8086 (C) ALE (C) Type 2 (C) 2 (C) 8-bit (1)	Date: 28-02-2018 Max Marks: 10M Signature of Invigilator  [ D) None [ D) None [ D) All [ D) None [	:: ] ] ]
SUB: MPMC   TIME: 20Min   Hall Ticket No:	nch: ECE & EEE  and data lines in 8086 (C) ALE (C) Type 2 (C) 2 (C) 8-bit (1)	Date: 28-02-2018  Max Marks: 10M  Signature of Invigilator  [ D) None  [ D) None  [ D) All  [	": " " " " " " " " " "
SUB: MPMC   TIME: 20Min   Hall Ticket No:	nch: ECE & EEE  and data lines in 8086 (C) ALE (C) Type 2 (C) 2 (C) 8-bit (C) Both A & B (1)	Date: 28-02-2018 Max Marks: 10M Signature of Invigilator  [ D) None	:: ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ;
SUB: MPMC   TIME: 20Min   Hall Ticket No:	nch: ECE & EEE  nd data lines in 8086 (C) ALE (1866) (C) Type 2 (1876) (C) 2 (1876) (C) 8-bit (1876) (C) Both A & B (1876) (C) 64 KB (1876)	Date: 28-02-2018  Max Marks: 10M  Signature of Invigilator  [ D) None	": " " " " " " " "
SUB: MPMC   TIME: 20Min   Hall Ticket No:	nch: ECE & EEE  and data lines in 8086 (C) ALE (C) ALE (C) Type 2 (C) 2 (C) 8-bit (C) Both A & B (C) 64 KB	Date: 28-02-2018 Max Marks: 10M Signature of Invigilator  [ D) None	": " " " " " " " " " " " " " " " " " "
SUB: MPMC   TIME: 20Min   Hall Ticket No:	nch: ECE & EEE  and data lines in 8086 (C) ALE (C) ALE (C) Type 2 (C) 2 (C) 8-bit (C) Both A & B (C) 64 KB (D) 64 KB	Date: 28-02-2018 Max Marks: 10M Signature of Invigilator  [ D) None [ [ D] None [ D] None [ [ D] None	"  1  1  1  1  1  1  1
SUB: MPMC   TIME: 20Min   Hall Ticket No:	nd data lines in 8086 (C) ALE (1866 (C) Type 2 (1876) (C) 8-bit (1876) (C) Both A & B (1876) (C) 64 KB (1876) (C) 64 KB (1876) (C) physical (1876) (d from lower nibble to upper	Date: 28-02-2018 Max Marks: 10M Signature of Invigilator  [ D) None [ [ D) None	" " " " " " " " " " " " " " " " " " "
SUB: MPMC   TIME: 20Min   Hall Ticket No:	nd data lines in 8086 (C) ALE (1866 (C) Type 2 (1876) (C) 8-bit (1876) (C) Both A & B (1876) (C) 64 KB (1876) (C) 64 KB (1876) (C) physical (1876) (d from lower nibble to upper	Date: 28-02-2018 Max Marks: 10M Signature of Invigilator  [ D) None [ [ D) None	": " " " " " " " " " " " " " " " "
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the correct answer:  1) pin separates the multiplexed address a (A) BHE' (B) MN/MX'  2) is a breakpoint interrupt in 808 (A) Type 0 (B) Type 3  3) 8086 operates in modes. (A) 1 (B) 3  4) What is the address bus size of 8086 (A) 16-bit (B) 20-bit  5) How many interrupts are there in 8086 (A) 256 (B) 00-FF h  6) Memory capacity of 8086 microprocessor (A) 512 KB (B) 2 MB  7) The index registers are used to hold a (A) Offset (B) Segment  8) Flag is set when the carry forwarded (A) Carry (B) Auxiliary carry  9) What is the size of offset address in 8086	nd data lines in 8086 (C) ALE (C) ALE (C) Type 2 (C) 2 (C) 8-bit (C) Both A & B (C) 64 KB (C) physical (C) physical (C) Parity (C) Parity (C) CO (C)	Date: 28-02-2018 Max Marks: 10M Signature of Invigilator  [ D) None [ [ D) None	": " " " " " " " " " " " " " " " " " "
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the correct answer:  1) pin separates the multiplexed address a (A) BHE' (B) MN/MX'  2) is a breakpoint interrupt in 808 (A) Type 0 (B) Type 3  3) 8086 operates in modes. (A) 1 (B) 3  4) What is the address bus size of 8086 (A) 16-bit (B) 20-bit  5) How many interrupts are there in 8086 (A) 256 (B) 00-FF h  6) Memory capacity of 8086 microprocessor (A) 512 KB (B) 2 MB  7) The index registers are used to hold a (A) Offset (B) Segment  8) Flag is set when the carry forwarded (A) Carry (B) Auxiliary carry  9) What is the size of offset address in 8086	nd data lines in 8086 (C) ALE (C) ALE (C) Type 2 (C) 2 (C) 8-bit (C) Both A & B (C) 64 KB (C) physical (D) physical (C) Parity (C) 18-bit	Date: 28-02-2018 Max Marks: 10M Signature of Invigilator  [ D) None [ [ D) None [ D) None [ [ D] None [ D] None [ [ D] None [ D]	" " " " " " " " " " " " " "

11) In PUSH instruction, after each execution of the instruction, the stack pointer is	[	]
(A) Incremented by 1 (B) Decremented by 1 (C) Decremented by 2 (D) None		
12) During comparison operation, the result of comparing or subtraction is stored	[	]
(A) Memory (B) Stack (C) Registers (D) No where		
13) The instruction that loads the AH register with the lower byte of the flag register is	[	]
(A)LAHF (B) SAHF (C) POPF (D) None		
14) The instruction is used for finding out the codes in case of code conversion problems is	[	]
(A) XCHG (B) XLAT (C) JCXZ (D) None		
15) The instruction, MOV AX, 0005H belongs to the address mode	[	]
(A) Direct (B) Indirect (C) Immediate (D) None		
16) If the offset of the operand is stored in one of the index registers, then it is	[	]
(A) Indirect (B) Indexed (C) Immediate (D) None		
17) The instruction that is not possible among the following is	[	]
(A) MOV AX, BX (B) MOV AX, [BX] (C) MOV 55H, AL (D) None		
18) The extension that is essential for every assembly level program is	[	]
(A) .ALP (B) .ASM (C) .ASP (D) None		
19) The directive that marks the end of a logical segment is	[	]
(A) ENDS (B) ENDP (C) END (D) None		
20) The ROR instruction rotates the contents of the destination operand to	[	]
(A) Left (B) Right (C) Right with Carry (D) None		
11) In PUSH instruction, after each execution of the instruction, the stack pointer is	[	]
(A) Incremented by 1 (B) Decremented by 1 (C) Decremented by 2 (D) None	r	,
12) During comparison operation, the result of comparing or subtraction is stored	L	]
(A) Memory (B) Stack (C) Registers (D) No where	r	1
13) The instruction that loads the AH register with the lower byte of the flag register is (A)LAHF (B) SAHF (C) POPF (D) None	L	]
14) The instruction is used for finding out the codes in case of code conversion problems is	[	]
(A) XCHG (B) XLAT (C) JCXZ (D) None		
15) The instruction, MOV AX, 0005H belongs to the address mode	[	]
(A) Direct (B) Indirect (C) Immediate (D) None		
16) If the offset of the operand is stored in one of the index registers, then it is	[	
(A) Indirect (B) Indexed (C) Immediate (D) None	F	]
17) The instruction that is not possible among the following is	Į	]
(A) MOV AX, BX (B) MOV AX, [BX] (C) MOV 55H, AL (D) None		]
18) The extension that is essential for every assembly level program is	_	]
(A) .ALP (B) .ASM (C) .ASP (D) None	[	]
	[	]
19) The directive that marks the end of a logical segment is	[	]
(A) ENDS (B) ENDP (C) END (D) None	[	]
	[ [	]



**SUB: MPMC** 

#### **G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY**

#### III B.Tech. II Sem., I MID Objective Exam

**Branch: ECE & EEE** 

Date: 28-02-2018

SET-3

TIME: 20Min Hall Ticket No:			Max Marks: 1 Signature of In	
	correct answer:			
	modes.			[
(A) 1	(B) 3	(C) 2	(D) All	
2) What is the address				[
(A) 16-bit	` '	(C) 8-bit	(D) None	
*	f offset address in 8086			[
(A) 16-bit	(B) 20-bit	(C) 18-bit	(D) None	
	of instruction Queue in 80			[ .
(A) 4 bytes	(B) 6 bytes	(C) 5 bytes	(D) None	
· · · · · · · · · · · · · · · · · · ·	pts are there in 8086			[
(A) 256	(-) * *	(C) Both A & B	(D) None	
	of 8086 microprocessor			[ .
(A) 512 KB	` '	(C) 64 KB	(D) None	
	rates the multiplexed address	ss and data lines in 8086		[
(A) BHE'	(B) MN/MX'	(C) ALE	(D) None	
8)	is a breakpoint interrupt in	8086		[
	(B) Type 3		(D) None	
9) The index register	s are used to hold	address		[
(A) Offset			(D) None	
10) Flag	g is set when the carry forw	arded from lower nibble	to upper nibble(D3 to D4)	[
	(B) Auxiliary carry		(D) None	
·	, , , , , , , , , , , , , , , , , , ,	• • •	,	
	G.PULLAIAH COLLEC		<u> </u>	
$GP\overline{CE}T$		II Sem., I MID Objective	e Exam	
Pioneering Innovative Education	<u>I</u>	Branch: ECE & EEE		
SUB: MPMC			Date: 28-02-20	18
TIME: 20Min			Max Marks: 1	0M
Hall Ticket No:			Signature of In	vigilator:

#### I - Choose the correct answer: 1) 8086 operates in modes. [ 1 (B)3(C) 2(D) All (A) 12) What is the address bus size of 8086 1 (B) 20-bit (A) 16-bit (C) 8-bit (D) None 3) What is the size of offset address in 8086 ſ ] (A) 16-bit (B) 20-bit (C) 18-bit (D) None 4) What is the length of instruction Queue in 8086 ] (A) 4 bytes (B) 6 bytes (C) 5 bytes (D) None 5) How many interrupts are there in 8086\_ 1 (B) 00-FF h (C) Both A & B (A) 256(D) None 6) Memory capacity of 8086 microprocessor 1 (B) 2 MB (A) 512 KB (C) 64 KB (D) None \_ pin separates the multiplexed address and data lines in 8086 7) ] (A) BHE (B) MN/MX' (C) ALE (D) None is a breakpoint interrupt in 8086 1 (A) Type 0 (C) Type 2 (D) None (B) Type 3 9) The index registers are used to hold \_ address 1 (A) Offset (B) Segment (C) physical (D) None Flag is set when the carry forwarded from lower nibble to upper nibble (D3 to D4) 10) \_\_\_\_\_ ] (A)Carry (B) Auxiliary carry (C) Parity (D) None

11) The instruction that (A)LAHF	t loads the AH register w (B) SAHF	rith the lower byte of the (C) POPF	flag register is (D) None	[	]
12) The instruction is a	used for finding out the co	odes in case of code conv	version problems is	Γ	]
(A) XCHG	(B) XLAT	(C) JCXZ	(D) None	L	,
, ,	marks the end of a logical	. ,		[	]
(A) ENDS	(B) ENDP	(C) END	(D) None		•
,	on rotates the contents of	* *	` ′	[	1
(A) Left	(B) Right	(C) Right with Carry	(D) None		•
` '	on, after each execution o	, , ,	` '	[	]
	1 (B) Decremented by 1	(C) Decremented by 2	(D) None		-
` '	n operation, the result of	` '	` '	[	]
(A) Memory	(B) Stack	(C) Registers	(D) No where		•
•	t is not possible among th	, , ,	( )	[	]
(A) MOV AX, BX	(B) MOV AX, [BX]	(C) MOV 55H, AL	(D) None		•
, ,	is essential for every ass	, ,	(= ) = 10000	ſ	1
(A) .ALP	(B) .ASM	(C) .ASP	(D) None	L	,
	OV AX, 0005H belongs	` '	(= ) = 10000	[	]
(A) Direct	(B) Indirect	(C) Immediate	(D) None	L	ı
,	operand is stored in one	* *	` '	[	]
(A) Indirect	(B) Indexed	(C) Immediate	(D) None	L	ı
(11) maneet	(b) mached	(C) immediate	(B) I tolle		
44) 771	. 1 . 1 . 1 . 1 . 1 . 1		CI.	-	-
11) The instruction that (A)LAHF	t loads the AH register w (B) SAHF	of the lower byte of the (C) POPF	flag register is (D) None	[	]
` '	used for finding out the co	` '		ſ	1
,	about the tribuling out the c	cass in case of code con	CIDIOII PIOOIOIIID ID		

(C) JCXZ

(C) END

(C) Right with Carry

(C) Decremented by 2

(C) MOV 55H, AL

(C) Registers

(C) .ASP

(C) Immediate

(C) Immediate

(A) XCHG

(A) ENDS

(A) Left

(A) Memory

(A) .ALP

(A) Direct

(A) Indirect

(A) MOV AX, BX

(B) XLAT

13) The directive that marks the end of a logical segment is

(B) ENDP

(B) Right

(B) Stack

(B) .ASM

(B) Indirect

(B) Indexed

17) The instruction that is not possible among the following is

(B) MOV AX, [BX]

19) The instruction, MOV AX, 0005H belongs to the address mode

18) The extension that is essential for every assembly level program is

(A) Incremented by 1 (B) Decremented by 1

14) The ROR instruction rotates the contents of the destination operand to

15) In PUSH instruction, after each execution of the instruction, the stack pointer is

16) During comparison operation, the result of comparing or subtraction is stored

20) If the offset of the operand is stored in one of the index registers, then it is

(D) None

(D) No where

1

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ſ

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# GPCET

### **G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY**

# III B.Tech. II Sem., I MID Objective Exam

**Branch: ECE & EEE** 

SET-4
-------

[

(D) None

]

TIME: 20Min Hall Ticket No:			Date: 28-02-2 Max Marks: Signature of	10M
I - Choose the				
_	of instruction Queue in 80			[
(A) 4 bytes		(C) 5 bytes	(D) None	
2) How many interrup	pts are there in 8086		(B) M	[
(A) 256	(B) 00-FF h	(C) Both A & B	(D) None	r
	is a breakpoint interrupt in		(D) None	l
(A) Type 0		(C) Type 2	(D) None	r
	s are used to hold		(D) None	L
(A) Offset		(C) physical	(D) None	r
	ates the multiplexed addres			L
* /	(B) MN/MX'	(C) ALE	(D) None	r
6) Flag 1	is set when the carry forwa			[
(A)Carry		(C) Parity	(D) None	г
/) 8080 operates in _	(B) 3	(C) 2	(D) A11	[
8) What is the addres		(C) 2	(D) All	г
· · · · · · · · · · · · ·		(C) 8-bit	(D) None	L
* /	of 8086 microprocessor	(C) 6-01t	(D) None	Г
(A) 512 KB	(B) 2 MB	(C) 64 KB	(D) None	[
` /	` '	(C) 04 KD	(D) None	г
(A) 16-bit	of offset address in 8086 (B) 20-bit	(C) 18-bit	(D) None	L
	~	~- ~		
CDCET.	G.PULLAIAH COLLEC			
GPCET Pioneering Innovative Education	III B.Tech.	II Sem., I MID Objectiv		SET-4
	III B.Tech.		ve Exam	
SUB: MPMC	III B.Tech.	II Sem., I MID Objectiv	<u>Ve Exam</u> Date: 28-02-2	2018
SUB: MPMC TIME: 20Min	III B.Tech.	II Sem., I MID Objectiv	Date: 28-02-2 Max Marks:	2018 10M
SUB: MPMC	III B.Tech.	II Sem., I MID Objectiv	<u>Ve Exam</u> Date: 28-02-2	2018 10M
SUB: MPMC TIME: 20Min Hall Ticket No:	III B.Tech.  E  correct answer:	II Sem., I MID Objectiv Branch: ECE & EEE	Date: 28-02-2 Max Marks:	2018 10M
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length	III B.Tech.  Ecorrect answer: of instruction Queue in 80	II Sem., I MID Objectiv Branch: ECE & EEE	Date: 28-02-2 Max Marks: Signature of	2018 10M
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length (A) 4 bytes	III B.Tech.  Ecorrect answer: of instruction Queue in 80 (B) 6 bytes	II Sem., I MID Objective Branch: ECE & EEE  86 (C) 5 bytes	Date: 28-02-2 Max Marks:	2018 10M Invigilator:
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length (A) 4 bytes 2) How many interrup	III B.Tech.  Ecorrect answer: of instruction Queue in 80 (B) 6 bytes pts are there in 8086	II Sem., I MID Objective Branch: ECE & EEE  86 (C) 5 bytes	Date: 28-02-2 Max Marks: Signature of	2018 10M
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length (A) 4 bytes 2) How many interruging (A) 256	III B.Tech.  Example 1  Correct answer:  of instruction Queue in 80  (B) 6 bytes pts are there in 8086  (B) 00-FF h	II Sem., I MID Objective Branch: ECE & EEE  86	Date: 28-02-2 Max Marks: Signature of	2018 10M Invigilator:
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the 6 1) What is the length (A) 4 bytes 2) How many interrug (A) 256 3)	correct answer: of instruction Queue in 80 (B) 6 bytes pts are there in 8086 (B) 00-FF h is a breakpoint interrupt in	II Sem., I MID Objective Branch: ECE & EEE  86	Date: 28-02-2 Max Marks: Signature of  (D) None  (D) None	2018 10M Invigilator:
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the 6 1) What is the length (A) 4 bytes 2) How many interrup (A) 256 3)i (A) Type 0	correct answer: of instruction Queue in 80 (B) 6 bytes pts are there in 8086 (B) 00-FF h is a breakpoint interrupt in (B) Type 3	II Sem., I MID Objective Branch: ECE & EEE  86	Date: 28-02-2 Max Marks: Signature of	2018 10M Invigilator:
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length (A) 4 bytes 2) How many interrup (A) 256 3) i	III B.Tech.  Ecorrect answer: of instruction Queue in 80 (B) 6 bytes pts are there in 8086 (B) 00-FF h is a breakpoint interrupt in (B) Type 3 s are used to hold	II Sem., I MID Objective Branch: ECE & EEE  86 (C) 5 bytes  (C) Both A & B 8086 (C) Type 2address	Date: 28-02-2 Max Marks: Signature of  (D) None  (D) None  (D) None	2018 10M Invigilator:
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length (A) 4 bytes 2) How many interrup (A) 256 3)i (A) Type 0 4) The index registers (A) Offset	III B.Tech.  Ecorrect answer: of instruction Queue in 80 (B) 6 bytes pts are there in 8086 (B) 00-FF h is a breakpoint interrupt in (B) Type 3 s are used to hold (B) Segment	II Sem., I MID Objective Branch: ECE & EEE  86	Date: 28-02-2 Max Marks: Signature of  (D) None (D) None (D) None (D) None	2018 10M Invigilator:
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length (A) 4 bytes 2) How many interrup (A) 256 3)i (A) Type 0 4) The index registers (A) Offset 5) pin separ	correct answer: of instruction Queue in 80 (B) 6 bytes pts are there in 8086 (B) 00-FF h is a breakpoint interrupt in (B) Type 3 s are used to hold (B) Segment ates the multiplexed address	86	Date: 28-02-2 Max Marks: Signature of  (D) None  (D) None  (D) None  (D) None	2018 10M Invigilator:
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length (A) 4 bytes 2) How many interrup (A) 256 3)	III B.Tech.  Ecorrect answer: of instruction Queue in 80 (B) 6 bytes pts are there in 8086 (B) 00-FF h is a breakpoint interrupt in (B) Type 3 s are used to hold (B) Segment	II Sem., I MID Objective Branch: ECE & EEE  86	Date: 28-02-2 Max Marks: Signature of  (D) None (D) None (D) None (D) None	2018 10M Invigilator:
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length (A) 4 bytes 2) How many interrup (A) 256 3) in (A) Type 0 4) The index registers (A) Offset 5) pin separ (A) BHE' 6) Flag in (A) Times (A) (B)	correct answer: of instruction Queue in 80 (B) 6 bytes pts are there in 8086 (B) 00-FF h is a breakpoint interrupt in (B) Type 3 s are used to hold (B) Segment ates the multiplexed address	II Sem., I MID Objective Branch: ECE & EEE  86 (C) 5 bytes  (C) Both A & B 8086 (C) Type 2 address (C) physical ss and data lines in 8086 (C) ALE	Date: 28-02-2 Max Marks: Signature of  (D) None (D) None (D) None (D) None (D) None	2018 10M Invigilator:
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length (A) 4 bytes 2) How many interrup (A) 256 3)	III B.Tech.  Ecorrect answer:  of instruction Queue in 80  (B) 6 bytes pts are there in 8086  (B) 00-FF h is a breakpoint interrupt in  (B) Type 3 s are used to hold  (B) Segment ates the multiplexed addres  (B) MN/MX' is set when the carry forwar  (B) Auxiliary carry	II Sem., I MID Objective Branch: ECE & EEE  86 (C) 5 bytes  (C) Both A & B 8086 (C) Type 2 address (C) physical ss and data lines in 8086 (C) ALE	Date: 28-02-2 Max Marks: Signature of  (D) None (D) None (D) None (D) None (D) None	2018 10M Invigilator:  [ [ [
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length (A) 4 bytes 2) How many interrup (A) 256 3)	III B.Tech.  Ecorrect answer: of instruction Queue in 80 (B) 6 bytes pts are there in 8086 (B) 00-FF h is a breakpoint interrupt in (B) Type 3 s are used to hold (B) Segment ates the multiplexed addres (B) MN/MX' is set when the carry forwa (B) Auxiliary carry modes.	II Sem., I MID Objective Branch: ECE & EEE  86 (C) 5 bytes  (C) Both A & B 8086 (C) Type 2 address (C) physical ss and data lines in 8086 (C) ALE rded from lower nibble to	Date: 28-02-2 Max Marks: Signature of  (D) None	2018 10M Invigilator:  [ [ [
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the case of the	III B.Tech.  Ecorrect answer: of instruction Queue in 80 (B) 6 bytes pts are there in 8086 (B) 00-FF h is a breakpoint interrupt in (B) Type 3 s are used to hold (B) Segment ates the multiplexed addres (B) MN/MX' is set when the carry forwar (B) Auxiliary carry modes. (B) 3	II Sem., I MID Objective Branch: ECE & EEE  86 (C) 5 bytes  (C) Both A & B 8086 (C) Type 2 address (C) physical ss and data lines in 8086 (C) ALE rded from lower nibble to	Date: 28-02-2 Max Marks: Signature of  (D) None	2018 10M Invigilator:  [ [ [ [
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length (A) 4 bytes 2) How many interrup (A) 256 3)	III B.Tech.  Ecorrect answer: of instruction Queue in 80 (B) 6 bytes pts are there in 8086 (B) 00-FF h is a breakpoint interrupt in (B) Type 3 s are used to hold (B) Segment ates the multiplexed addres (B) MN/MX' is set when the carry forwar (B) Auxiliary carry modes. (B) 3	86	Date: 28-02-2 Max Marks: Signature of  (D) None	2018 10M Invigilator:  [ [ [ [
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length (A) 4 bytes 2) How many interrup (A) 256 3)i (A) Type 0 4) The index registers (A) Offset 5) pin separ (A) BHE' 6) Flag in (A)Carry 7) 8086 operates in (A) 1 8) What is the addres (A) 16-bit	III B.Tech.  In It B.Tech.  In It B.Tech.  In It B.Tech.  In It B.Tech.  It B.	86	Date: 28-02-2 Max Marks: Signature of  (D) None	2018 10M Invigilator:  [ [ [ [
SUB: MPMC TIME: 20Min Hall Ticket No:  I - Choose the (1) What is the length (A) 4 bytes 2) How many interrup (A) 256 3)	Correct answer: of instruction Queue in 80 (B) 6 bytes pts are there in 8086 (B) 00-FF h is a breakpoint interrupt in (B) Type 3 s are used to hold (B) Segment ates the multiplexed addres (B) MN/MX' is set when the carry forwa (B) Auxiliary carry modes. (B) 3 s bus size of 8086	II Sem., I MID Objective Branch: ECE & EEE  86	Date: 28-02-2 Max Marks: Signature of  (D) None	2018 10M Invigilator:  [ [ [ [

(C) 18-bit

10) What is the size of offset address in 8086

(B) 20-bit

(A) 16-bit

11) The instruction that is not possible among the following is	[	]
(A) MOV AX, BX (B) MOV AX, [BX] (C) MOV 55H, AL (D) None		
12) The extension that is essential for every assembly level program is	[	]
(A) .ALP (B) .ASM (C) .ASP (D) None		
13) The directive that marks the end of a logical segment is	[	]
(A) ENDS (B) ENDP (C) END (D) None		
14) The ROR instruction rotates the contents of the destination operand to	[	]
(A) Left (B) Right (C) Right with Carry (D) None		
15) The instruction, MOV AX, 0005H belongs to the address mode	[	]
(A) Direct (B) Indirect (C) Immediate (D) None		
16) If the offset of the operand is stored in one of the index registers, then it is	[	]
(A) Indirect (B) Indexed (C) Immediate (D) None	_	
17) The instruction that loads the AH register with the lower byte of the flag register is (A)LAHF (B) SAHF (C) POPF (D) None	[	]
18) The instruction is used for finding out the codes in case of code conversion problems is	ſ	]
(A) XCHG (B) XLAT (C) JCXZ (D) None		-
19) In PUSH instruction, after each execution of the instruction, the stack pointer is	[	]
(A) Incremented by 1 (B) Decremented by 1 (C) Decremented by 2 (D) None	·	•
20) During comparison operation, the result of comparing or subtraction is stored	[	]
(A) Memory (B) Stack (C) Registers (D) No where	L	,
11) The instruction that is not possible among the following is	[	1
(A) MOV AX, BX (B) MOV AX, [BX] (C) MOV 55H, AL (D) None	L	,
12) The extension that is essential for every assembly level program is	[	]
(A) .ALP (B) .ASM (C) .ASP (D) None	·	•
13) The directive that marks the end of a logical segment is	[	]
(A) ENDS (B) ENDP (C) END (D) None		_
14) The ROR instruction rotates the contents of the destination operand to	[	]
(A) Left (B) Right (C) Right with Carry (D) None	-	-
15) The instruction, MOV AX, 0005H belongs to the address mode	[	]
(A) Direct (B) Indirect (C) Immediate (D) None		
16) If the offset of the operand is stored in one of the index registers, then it is	[	]
(A) Indirect (B) Indexed (C) Immediate (D) None		
17) The instruction that loads the AH register with the lower byte of the flag register is	[	]
(A)LAHF (B) SAHF (C) POPF (D) None		
18) The instruction is used for finding out the codes in case of code conversion problems is	[	]
(A) XCHG (B) XLAT (C) JCXZ (D) None		
19) In PUSH instruction, after each execution of the instruction, the stack pointer is	[	]
(A) Incremented by 1 (B) Decremented by 1 (C) Decremented by 2 (D) None		
20) During comparison operation, the result of comparing or subtraction is stored	[	]
(A) Memory (B) Stack (C) Registers (D) No where		