G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) **SET-1**

III B.Tech.II SEM, I MID Objective Exam Branch: ECE

Sub: VLSI Design **Date : 6-03-18**

Time: 20 min **Max.Marks:10**

Roll No: **Invigilator signature:**

1. Length of the channel should be at least 4d. [T/F]
2. The other name for resistive region is saturation region [T/F]
3. The ratio of g_m / c_g gives trans conductance [T/F]
4. When red color crosses green N-MOSFET is formed [T/F]
5. Rise time is slower than fall time by a factor of 2.5. [T/F]
6. As die size shrinks ,the complexity of photo masks gets _____
7. Contact used to connect gate and source in D-MOSFET is_____
8. The source of pMOS in CMOS inverter is connected to_____
9. To distinguish pMOS & nMOS transistors _____ line is used in CMOS logic.
10. Equation for Drain current in saturation region, I_{ds} = _____

11. Implant	[ ]	a. Black	
12. Metal -2	[ ]	b. Yellow	
13. Diffusion (p active)	[ ]	c. Red	
14. Polysilicon -1	[ ]	d. Green	
15. Contact cut	[ ]	e. Purple	

16. Problem that arises in CMOS circuits [ ]
    a. latch up b.body effect c.CLM d.feed back

17. The condition Vgs>Vt, Vds<Vgs-Vt represents the region [ ]
    a. saturation b. active c. cutoff d. linear region

18. Total inverter delay for a pair of nMOS inverters is [ ]
    a.2τ b.3 τ c.4 τ d.5 τ

19. Sheet resistance of n-channel transistor [ ]
    a.$2x10^4$ Ω b. $2.5x10^4$ Ω c. $3x10^4$ Ω d. 10^4 Ω

20. The product of electron mobility with electric field gives [ ]
    a. Current b. Voltage c. Velocity d. Time

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12. Metal -2	[ ]	b. Yellow	
13. Diffusion (p active)	[ ]	c. Red	
14. Polysilicon -1	[ ]	d. Green	
15. Contact cut	[ ]	e. Purple	

16. Problem that arises in CMOS circuits [ ]
    a. latch up b.body effect c.CLM d.feed back

17. The condition Vgs>Vt, Vds<Vgs-Vt represents the region [ ]
    a. saturation b. active c. cutoff d. linear region

18. Total inverter delay for a pair of nMOS inverters is [ ]
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    a.$2x10^4$ Ω b. $2.5x10^4$ Ω c. $3x10^4$ Ω d. 10^4 Ω

20. The product of electron mobility with electric field gives [ ]
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G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) **SET-2**

III B.Tech.II SEM, I MID Objective Exam Branch: ECE

Sub: VLSI Design **Date : 6-03-18**

Time: 20 min **Max.Marks:10**

Roll No: **Invigilator signature:**

1. Length of the channel should be at least 4d. [T/F]
2. The other name for resistive region is saturation region [T/F]
3. The ratio of g_m / c_g gives trans conductance [T/F]
4. When red color crosses green N-MOSFET is formed [T/F]
5. Rise time is slower than fall time by a factor of 2.5. [T/F]
6. Problem that arises in CMOS circuits [ ]
   a. latch up b.body effect c.CLM d.feed back

2. The condition Vgs>Vt, Vds<Vgs-Vt represents the region [ ]
   a. saturation b. active c. cutoff d. linear region

3. Total inverter delay for a pair of nMOS inverters is [ ]
   a.2τ b.3 τ c.4 τ d.5 τ

4. Sheet resistance of n-channel transistor [ ]
   a.$2x10^4$ Ω b. $2.5x10^4$ Ω c. $3x10^4$ Ω d. 10^4 Ω

5. The product of electron mobility with electric field gives [ ]
   a. Current b. Voltage c. Velocity d. Time

6. Implant	[ ]	a. Black
7. Metal -2	[ ]	b. Yellow
8. Diffusion (p active)	[ ]	c. Red
9. Polysilicon -1	[ ]	d. Green
10. Contact cut	[ ]	e. Purple

11. As die size shrinks ,the complexity of photo masks gets _____
12. Contact used to connect gate and source in D-MOSFET is_____
13. The source of pMOS in CMOS inverter is connected to_____
14. To distinguish pMOS & nMOS transistors _____ line is used in CMOS logic.
15. Equation for Drain current in saturation region, I_{ds} = _____

G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) **SET-2**

III B.Tech.II SEM, I MID Objective Exam Branch: ECE

Sub: VLSI Design **Date : 6-03-18**

Time: 20 min **Max.Marks:10**

Roll No: **Invigilator signature:**

1. Problem that arises in CMOS circuits [ ]
   a. latch up b.body effect c.CLM d.feed back

2. The condition Vgs>Vt, Vds<Vgs-Vt represents the region [ ]
   a. saturation b. active c. cutoff d. linear region

3. Total inverter delay for a pair of nMOS inverters is [ ]
   a.2τ b.3 τ c.4 τ d.5 τ

4. Sheet resistance of n-channel transistor [ ]
   a.$2x10^4$ Ω b. $2.5x10^4$ Ω c. $3x10^4$ Ω d. 10^4 Ω

5. The product of electron mobility with electric field gives [ ]
   a. Current b. Voltage c. Velocity d. Time

6. Implant	[ ]	a. Black
7. Metal -2	[ ]	b. Yellow
8. Diffusion (p active)	[ ]	c. Red
9. Polysilicon -1	[ ]	d. Green
10. Contact cut	[ ]	e. Purple

11. As die size shrinks ,the complexity of photo masks gets _____
12. Contact used to connect gate and source in D-MOSFET is_____
13. The source of pMOS in CMOS inverter is connected to_____
14. To distinguish pMOS & nMOS transistors _____ line is used in CMOS logic.
15. Equation for Drain current in saturation region, I_{ds} = _____

16. Length of the channel should be at least 4d. [T/F]
17. The other name for resistive region is saturation region [T/F]
18. The ratio of g_m / c_g gives trans conductance [T/F]
19. When red color crosses green N-MOSFET is formed [T/F]
20. Rise time is slower than fall time by a factor of 2.5. [T/F]

G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) **SET-3**

III B.Tech.II SEM, I MID Objective Exam Branch: ECE

Sub: VLSI Design **Date : 6-03-18**

Time: 20 min **Max.Marks:10**

Roll No: **Invigilator signature:**

1. Implant [ ] a. Black
2. Metal -2 [ ] b. Yellow
3. Diffusion (p active) [ ] c. Red
4. Polysilicon -1 [ ] d. Green
5. Contact cut [ ] e. Purple

6. Length of the channel should be at least 4d. [T/F]
7. The other name for resistive region is saturation region [T/F]
8. The ratio of g_m / c_g gives trans conductance [T/F]
9. When red color crosses green N-MOSFET is formed [T/F]
10. Rise time is slower than fall time by a factor of [T/F]
11. Problem that arises in CMOS circuits [ ]
    a. latch up b.body effect c.CLM d.feed back
12. The condition Vgs>Vt, Vds<Vgs-Vt represents the region [ ]
    a. saturation b. active c. cutoff d. linear region
13. Total inverter delay for a pair of nMOS inverters is [ ]
    a.2τ b.3 τ c.4 τ d.5 τ
14. Sheet resistance of n-channel transistor [ ]
    a.$2x10^4$ Ω b. $2.5x10^4$ Ω c. $3x10^4$ Ω d. 10^4 Ω
15. The product of electron mobility with electric field gives [ ]
    a. Current b. Voltage c. Velocity d. Time
16. As die size shrinks ,the complexity of photo masks gets _____
1. Contact used to connect gate and source in D-MOSFET is_____
2. The source of pMOS in CMOS inverter is connected to_____
3. To distinguish pMOS & nMOS transistors _____ line is used in CMOS logic.
4. Equation for Drain current in saturation region, I_{ds} = _____

G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) **SET-3**

III B.Tech.II SEM, I MID Objective Exam Branch: ECE

Sub: VLSI Design **Date : 6-03-18**

Time: 20 min **Max.Marks:10**

Roll No: **Invigilator signature:**

1. Implant [ ] a. Black
2. Metal -2 [ ] b. Yellow
3. Diffusion (p active) [ ] c. Red
4. Polysilicon -1 [ ] d. Green
5. Contact cut [ ] e. Purple

6. Length of the channel should be at least 4d. [T/F]
7. The other name for resistive region is saturation region [T/F]
8. The ratio of g_m / c_g gives trans conductance [T/F]
9. When red color crosses green N-MOSFET is formed [T/F]
10. Rise time is slower than fall time by a factor of [T/F]
11. Problem that arises in CMOS circuits [ ]
    a. latch up b.body effect c.CLM d.feed back
12. The condition Vgs>Vt, Vds<Vgs-Vt represents the region [ ]
    a. saturation b. active c. cutoff d. linear region
13. Total inverter delay for a pair of nMOS inverters is [ ]
    a.2τ b.3 τ c.4 τ d.5 τ
14. Sheet resistance of n-channel transistor [ ]
    a.$2x10^4$ Ω b. $2.5x10^4$ Ω c. $3x10^4$ Ω d. 10^4 Ω
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16. As die size shrinks ,the complexity of photo masks gets _____
17. Contact used to connect gate and source in D-MOSFET is_____
18. The source of pMOS in CMOS inverter is connected to_____
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G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) **SET-4**

III B.Tech.II SEM, I MID Objective Exam Branch: ECE

Sub: VLSI Design **Date : 6-03-18**

Time: 20 min **Max.Marks:10**

Roll No: **Invigilator signature:**

1. As die size shrinks ,the complexity of photo masks gets _____
2. Contact used to connect gate and source in D-MOSFET is_____
3. The source of pMOS in CMOS inverter is connected to_____
4. To distinguish pMOS & nMOS transistors _____ line is used in CMOS logic.
5. Equation for Drain current in saturation region, I_{ds} = _____
6. Length of the channel should be at least 4d. [T/F]
7. The other name for resistive region is saturation region [T/F]
8. The ratio of g_m /c_g gives trans conductance [T/F]
9. When red color crosses green N-MOSFET is formed [T/F]
10. Rise time is slower than fall time by a factor of 2.5. [T/F]
11. Implant [ ] a. Black
12. Metal -2 [ ] b. Yellow
13. Diffusion (p active) [ ] c. Red
14. Polysilicon -1 [ ] d. Green
15. Contact cut [ ] e. Purple
16. Problem that arises in CMOS circuits [ ]
    a. latch up b.body effect c.CLM d.feed back
17. The condition Vgs>Vt, Vds<Vgs-Vt represents the region [ ]
    a. saturation b. active c. cutoff d. linear region
18. Total inverter delay for a pair of nMOS inverters is [ ]
    a.2τ b.3 τ c.4 τ d.5 τ
19. Sheet resistance of n-channel transistor [ ]
    a.$2x10^4$ Ω b. $2.5x10^4$ Ω c. $3x10^4$ Ω d. 10^4 Ω
20. The product of electron mobility with electric field gives [ ]
    a. Current b. Voltage c. Velocity d. Time

G.PULLAIAH COLLEGE OF ENGINEERING & TECHNOLOGY (AT) **SET-4**

III B.Tech.II SEM, I MID Objective Exam Branch: ECE

Sub: VLSI Design **Date : 6-03-18**

Time: 20 min **Max.Marks:10**

Roll No: **Invigilator signature:**

1. As die size shrinks ,the complexity of photo masks gets _____
2. Contact used to connect gate and source in D-MOSFET is_____
3. The source of pMOS in CMOS inverter is connected to_____
4. To distinguish pMOS & nMOS transistors _____ line is used in CMOS logic.
5. Equation for Drain current in saturation region, I_{ds} = _____
6. Length of the channel should be at least 4d. [T/F]
7. The other name for resistive region is saturation region [T/F]
8. The ratio of g_m /c_g gives trans conductance [T/F]
9. When red color crosses green N-MOSFET is formed [T/F]
10. Rise time is slower than fall time by a factor of 2.5. [T/F]
11. Implant [ ] a. Black
12. Metal -2 [ ] b. Yellow
13. Diffusion (p active) [ ] c. Red
14. Polysilicon -1 [ ] d. Green
15. Contact cut [ ] e. Purple
16. Problem that arises in CMOS circuits [ ]
    a. latch up b.body effect c.CLM d.feed back
17. The condition Vgs>Vt, Vds<Vgs-Vt represents the region [ ]
    a. saturation b. active c. cutoff d. linear region
18. Total inverter delay for a pair of nMOS inverters is [ ]
    a.2τ b.3 τ c.4 τ d.5 τ
19. Sheet resistance of n-channel transistor [ ]
    a.$2x10^4$ Ω b. $2.5x10^4$ Ω c. $3x10^4$ Ω d. 10^4 Ω
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    a. Current b. Voltage c. Velocity d. Time