RF INTEGRATED CIRCUITS: NOTES

UNIT-4

RF POWER AMPLIFIERS

1. CLASS A AMPLIFIERS:- The Class A power amplifier is small-signal amplifier as shown in figure 1 The assumption in Class A power amplifier design is that bias levels are chosen so that the transistor operates (quasi)Linearly. For a bipolar realization this condition is satisfied by avoiding cutoff and saturation for MOS implementations the transistor is kept in the pentode (“saturation") region of operation. The primary distinction between Class A power amplifiers and small-signal amplifiers is that the signal currents ill a PA arc a substantial fraction of the bias level and one would therefore expect potentially serious distortion. In narrowband operation as implied by the general circuit model, a tank circuit solves the distortion problem potentially associated with such large swings so that overall linear operation prevails. Although linearity is certainly desirable, the Class A amplifier provides it at the expense of efficiency because there is always dissipation due to the bias current, even when there is no signal. To understand quantitatively why the efficiency is poor, assume that the drain current is reasonably well approximated by

$$i_D = I_{DC} + i_{rf} \sin \omega_0 t. \tag{1}$$

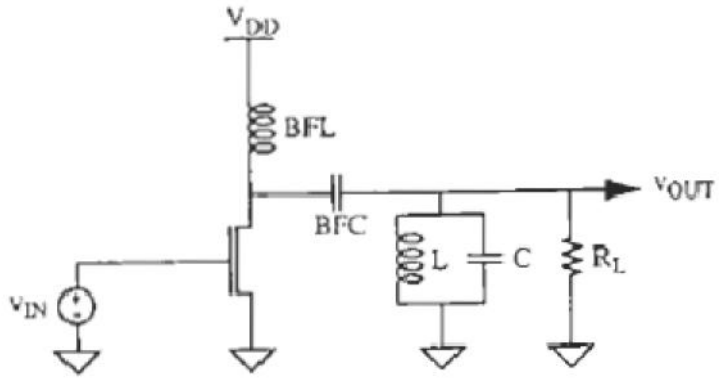


Fig 1. General pawer amplifier model.

where *IDC* is the bias current *irs* is the amplitude of the signal component of the drain current and *Wo* is the signal frequency (and also the resonant frequency of the tank).

The output voltage is simply the product of a signal current and the load resistance. Since the big fat inductor *BFL* forces a substantially constant current through it, KCL tells us that the signal current is none other than the signal component of the drain current. Therefore,

$$v_o = -i_{rf} R \sin \omega_0 t. \tag{2}$$

Finally the drain voltage is the sum of the DC drain voltage and the signal voltage. The big fat inductor *BFL* presents a DC short. so the drain voltage swings symmetrically about *VDD* The drain voltage and current are therefore offset sinusoids that arc 180^0 out of phase with each other, as shown in Figure 1.2.

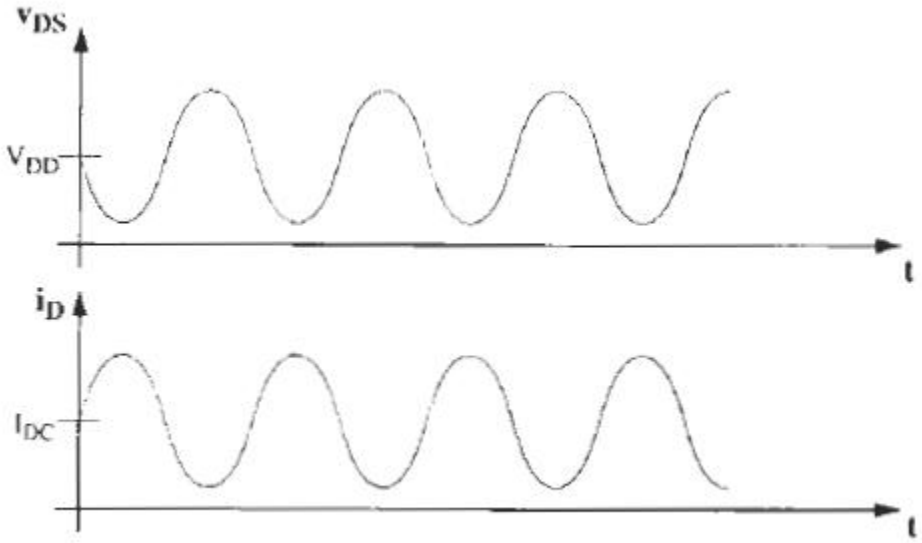


Fig1.2 Drain voltage and current for ideal class A amplifier.

it should be clear from the figure that the transistor always dissipates power because the product of drain current and drain voltage is always positive. To evaluate this dissipation quantitatively, compute the efficiency by first calculating the signal power delivered to the resistor *R* is given by

$$P_{rf} = \frac{i_{rf}^2 R}{2}. \tag{3}$$

Next compute the DC power supplied to the amplifier. Let us assume that the quiescent drain current IDC is made just large enough to guarantee that the transistor does not ever cut off. That is

$$I_{DC} = i_{rf}, \tag{4}$$

so that the input DC power is

$$P_{DC} = I_{DC} V_{DD} = i_{rf} V_{DD}. \tag{5}$$

The ratio of RF output power to DC input power is a measure of efficiency (usually called the drain efficiency) and is given by

$$\eta \equiv \frac{P_{rf}}{P_{DC}} = \frac{i_{rf}^2 (R/2)}{i_{rf} V_{DD}} = \frac{i_{rf} R}{2V_{DD}}. \tag{6}$$

Now the absolute maximum that the product *irsR* can have is *VDD* Therefore. The maximum theoretical drain efficiency is just 50%. If one makes due allowance for nonzero minimum *VDS* variation in bias conditions. Non ideal drive amplitude, and inevitable losses in the filter and interconnect, values substantially smaller than 50% often result - particularly at lower supply voltages, where *VDS on* represents a larger fraction of *VDD*. Consequently, drain efficiencies of *30%--35%* are not at all unusual for practical Class A amplifiers.

Aside from efficiency, another important consideration is the stress on the output transistor. In a Class A amplifier, the maximum drain-to-source voltage is *2VDD* while the peak drain current has a value of *2VDD/R*. Hence, the device must be able to withstand peak voltages and currents of these magnitudes, even though both maxima do not occur simultaneously. Since scaling trends in IC process technology force reductions in breakdown voltage, the design of PAs becomes more difficult with each passing generation.

One common way to quantify the relative stress on the devices is to define another type of efficiency, called the "normalized power output capability:' which is simply the ratio of the actual output power to the product of the maximum device voltage and current. For this type of amplifier, the maximum value of this dimensionless figure of merit is

$$P_N \equiv \frac{P_{rf}}{v_{DS,pk} i_{D,max}} = \frac{V_{DD}^2/(2R)}{(2V_{DD})(2V_{DD}/R)} = \frac{1}{8}. \tag{8}$$

The Class A amplifier thus provides linearity at the cost of low efficiency and relatively large device stresses. For this reason, Class A amplifiers are rare in RF power applications" and relatively rare in audio power applications.

It is important to underscore once again that the 50% efficiency value represents an upper limit. If the drain swing is less than the maximum assumed in the foregoing and if there are additional losses anywhere else, the efficiency drops. As the swing approaches zero, the drain efficiency also approaches zero because the signal power delivered to the load goes to zero while the transistor continues to burn DC power.

2. CLASS B AMPLIFIERS:- In the Class B amplifier, the bias is arranged to shut off the output device half of every cycle. An exact 50% conduction duty cycle is a mathematical point so that true Class B amplifiers do not actually exist. However, we must distinguish between distortion in the output (an earmark of nonlinearity) and proportionality, or lack thereof, between input and output powers (evaluated at the fundamental). A single-ended Class B amplifier may produce a non sinusoidal output but still act linearly in this sense of input-output power proportionality, We still care about out-of-band spectral components, and a *high-Q* resonator is absolutely mandatory in order to obtain an acceptable approximation to a sinusoidal output voltage.

Although the single-transistor version of a Class B amplifier is what we'll analyze here, it should be mentioned that most practical Class B amplifiers are push-pull configurations of two transistors.

For this amplifier, then, we assume that the drain current is sinusoidal for one half-cycle and zero for the other half-cycle is

$$i_D = i_{rf} \sin \omega_0 t \quad \text{for } i_D > 0. \tag{1}$$

The output tank filters out the harmonics of this current, leaving a sinusoidal drain voltage as in the Class A amplifier. The drain current and drain voltage therefore appear approximately as shown in Figure 1.

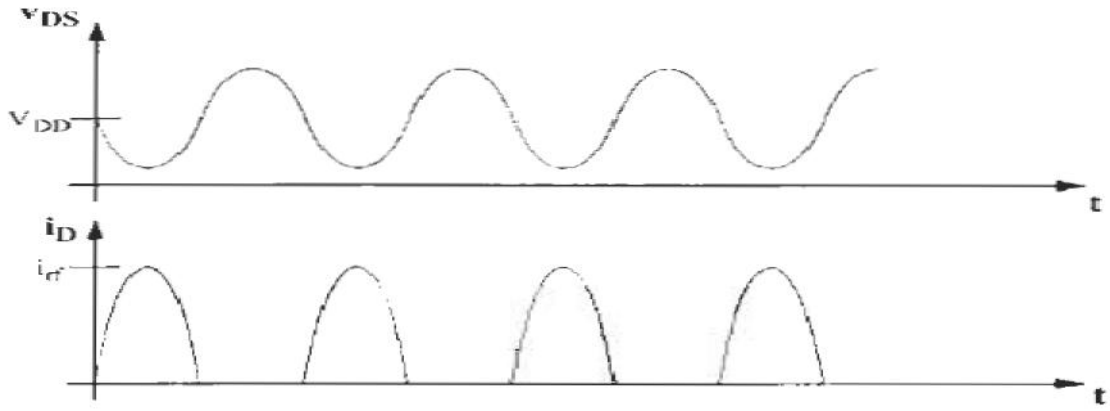


Fig 1. Drain voltage and current for ideal Class B amplifier

$$i_{fund} = \frac{2}{T} \int_0^{T/2} i_{rf} (\sin \omega_0 t)(\sin \omega_0 t)\, dt = \frac{i_{rf}}{2},$$

$$v_{out} \approx \frac{i_{rf}}{2} R \sin \omega_0 t. \tag{2),(3)}$$

Since the maximum possible value of Vout is *VDD.* it is clear from Eqn. 3 that the maximum value of *irf* is

$$i_{rf,\max} = \frac{2V_{DD}}{R}.$$

(4)

The peak drain current and maximum output voltage are therefore the same as for the Class A amplifier.

Computing the drain efficiency as before we first calculate the output power as follows

$$P_o = \frac{v_o^2}{2R},$$

(5)

Where *Vo* is the amplitude of the signal across the load resistor. The maximum value of the amplitude remains *VDD.* so the maximum output power is

$$P_{o,\max} = \frac{V_{DD}^2}{2R}.$$

(6)

Computing the DC input power requires computation of the average drain current is given by

$$\overline{i_D} = \frac{1}{T}\int_0^{T/2} \frac{2V_{DD}}{R} \sin \omega_0 t \, dt = \frac{2V_{DD}}{\pi R}.$$

(7)

so that the DC power supplied is

$$P_{DC} = \frac{2V_{DD}^2}{\pi R}.$$

Finally, the maximum drain efficiency for a Class B amplifier is

$$\eta = \frac{P_{o,\max}}{P_{DC}} = \frac{\pi}{4} \approx 0.785.$$

(8),(9)

The drain efficiency is thus considerably higher than for the Class A PA. Continuing with our hypothetical example of a 50-kW transmitter, the device dissipation would diminish to less than one third of its previous value, from 50 kW to under 14 kW. However, as with the Class A amplifier the actual efficiency of any practical implementation will be somewhat lower than given by this analysis owing to effects that we have

neglected. It remains true that, all other things held equal, the Class B amplifier offers substantially higher efficiency than its Class A PA.

The normalized power capability of this amplifier is 1/8 the same as for the Class A, since the output power maximum drain voltage and maximum drain current are the same.

3. THE CLASS C AMPLIFIER:- In a Class C PA, the gate bias is arranged to cause the transistor to conduct less than half the time. Consequently, the drain current consists of a periodic train of pulses. It is traditional to approximate these pulses by the top pieces of sinusoids to facilitate a direct analysis. Specifically, one assumes that the drain current is of the following form is given by

$$i_D = I_{DC} + i_{rf} \sin \omega_0 t, \quad i_D > 0, \tag{1}$$

where the offset *I*DC which is analogous to the bias current in a linear amplifier, is actually negative for a Class C amplifier. Of course, the *overall* drain current *iD* is always positive or zero. That is, the drain current is a piece of a sine wave when the transistor is active and zero when the transistor is in cutoff. We continue to assume that the transistor behaves at all times as a current source which is having high output impedance.

Because we still have a high-Q output tank, the voltage across the load remains substantially sinusoidal. The drain voltage and drain current therefore appear as depicted in Figure 1.

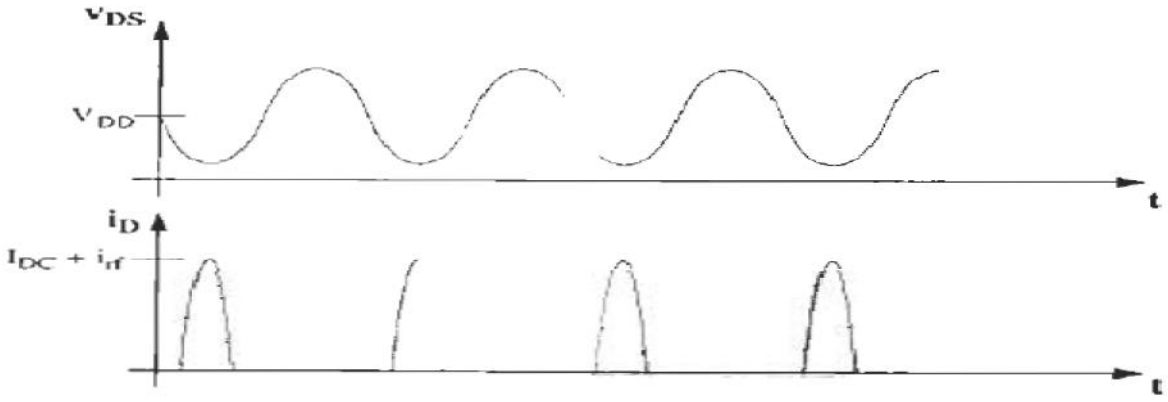
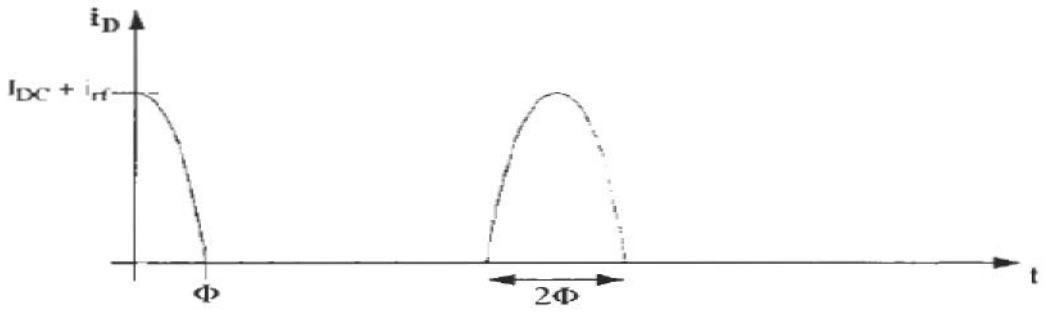


Fig 1. Drain voltage and current for ideal Class C amplifier

We begin by solving for the total angle over which the drain current is nonzero. In order to reduce the number of steps needed to arrive at the answer, we first rewrite the expression for the drain current in terms of a cosine rather than a sine is

$$i_D = I_{DC} + i_{rf} \cos \omega_0 t, \quad i_D > 0. \tag{1}$$

With this modification, the current pulses appear as shown in Figure 2.



Setting the current equal to zero and solving for the total conduction angle 2¢ yields

$$2\Phi = 2 \cdot \cos^{-1}\left(-\frac{I_{DC}}{i_{rf}}\right). \tag{2}$$

which may be solved for the "bias current" as follows:

$$I_{DC} = -i_{rf} \cos \Phi.$$

We are now in a position to compute the average drain current:

$$\overline{i_D} = \frac{1}{2\pi} \int_{-\Phi}^{\Phi} (I_{DC} + i_{rf} \cos \phi)\, d\phi = \frac{1}{2\pi} 2\phi I_{DC} + \frac{1}{2\pi} [i_{rf} \sin \phi] \Big|_{-\Phi}^{\Phi}.$$

After substitution with the expression for I_{DC}, this yields:

$$I_{DC} = \frac{i_{rf}}{\pi} [\sin \Phi - \Phi \cos \Phi].$$

We will use this expression shortly in deriving an equation for the efficiency function of conduction angle. (3)(4)(5)

The other quantity we need is a general expression for the power delivered to the load. As with the Class B case, this derivation is simplified because of the high-Q tank circuit, so we need to compute only the fundamental term in the Fourier series is given by

$$i_{\text{fund}} = \frac{2}{T}\int_0^T i_D \cos\omega_0 t\, dt = \frac{1}{2\pi}(4I_{DC}\sin\Phi + 2i_{rf}\Phi + i_{rf}\sin 2\Phi).$$

Substituting for I_{DC}, we obtain

$$i_{\text{fund}} = \frac{i_{rf}}{2\pi}(2\Phi - \sin 2\Phi). \tag{6)(7}$$

With our expression for the fundamental current through the load, we can derive an equation for the maximum output voltage swing:

$$V_{DD} = i_{rf}\frac{R}{2\pi}(2\Phi - \sin 2\Phi),$$

allowing us to solve for the current i_{rf} in terms of V_{DD}:

$$i_{rf} = \frac{2\pi V_{DD}}{R(2\Phi - \sin 2\Phi)}. \tag{8)(9}$$

The peak drain current is the sum of i_{rf} and the bias term:

$$i_{D,\text{pk}} = \frac{i_{rf}}{\pi}[\sin\Phi - \Phi\cos\Phi] + \frac{2\pi V_{DD}}{R(2\Phi - \sin 2\Phi)},$$

which simplifies to

$$i_{D,\text{pk}} = \frac{2\pi V_{DD}}{R(2\Phi - \sin 2\Phi)}\left[1 + \frac{(\sin\Phi - \Phi\cos\Phi)}{\pi}\right]. \tag{10)(11}$$

For a fixed output voltage, the peak drain current approaches infinity as the pulsewidth decreases toward zero.

The drain efficiency is readily calculated with the equations we've just derived that is given by

$$\eta_{\max} = \frac{2\Phi - \sin 2\Phi}{4(\sin\Phi - \Phi\cos\Phi)}. \tag{12}$$

As the conduction angle shrinks toward zero, the efficiency approaches 100o/c. While this sounds promising, the gain and output power unfortunately also tend toward zero at the same time, since the fundamental component in the ever-narrowing slivers of drain current shrinks as well. Furthermore, it is clear from the equation for peak drain current that the normalized power-handling capability of the Class C amplifier approaches zero as the conduction angle approaches zero. All of these tradeoffs force the attainment of less than 100% efficiency in practice, since we generally want a reasonable amount of output power as well as high efficiency.

4. THE CLASS AS AMPLIFIER:- The Class AB amplifier, as its name suggests, conducts somewhere between 50% and 100% of a cycle, depending on the bias levels chosen. As a result, its efficiency and linearity are intermediate between those of a Class A and Class B amplifier.

We do not need to undertake a separate derivation of equations for this amplifier because the equations for the Class C case also apply here (they also include the Class A and Class B case). The only difference is that the bias current is positive, rather than negative.

The PAs presented so far use the active device as a controlled current source. Another approach is to use the device as a switch, the reasoning being that a switch ideally dissipates no power, for there is either zero voltage across it or zero current through it. Since the switch's *V-I* product is therefore always zero, the transistor dissipates no power and the efficiency must be 100%.

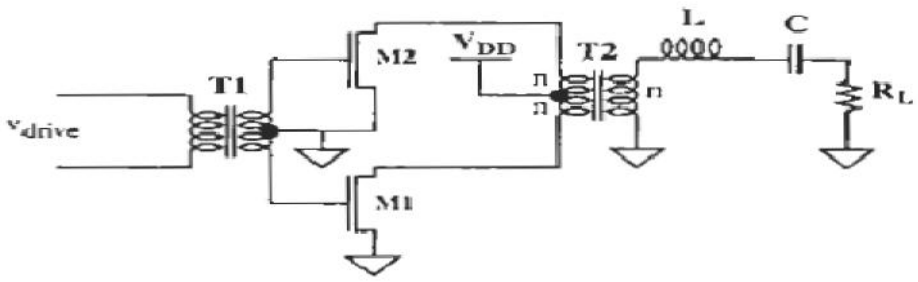


Fig1. Class D amplifier

As shown in Figure 1 it looks the same as a push-pull, transformer-coupled version of a Class B amplifier. In contrast with the parallel tanks we've typically seen, a series *RLC* network is used in the output of this amplifier.

The input connection guarantees that only one transistor is driven on at a given time, with one transistor handling the positive half-cycles and the other the negative half-cycles, just as in a push-pull Class B. The difference here is that the transistors are driven hard enough to make them act like switches, rather than as linear (or quasi linear) amplifiers.

Because of the switching action, each primary terminal of the output transformer *T2* is alternately driven to ground, yielding a square-wave voltage across the primary (and therefore across the secondary) winding. When one drain goes to zero volts, transformer action forces the other drain to a voltage of 2V*DD*. The output filter allows only the fundamental component of this square wave to flow into the load.

Since only fundamental currents flow in the secondary circuit, the primary current is sinusoidal as well. As a consequence, each switch sees a sinusoid for the half-cycle that it is on, and the transformer current and voltage therefore appear as in Figures 2 and 3. Because the transistors act like switches the theoretical efficiency of the Class D amplifier is 100%.

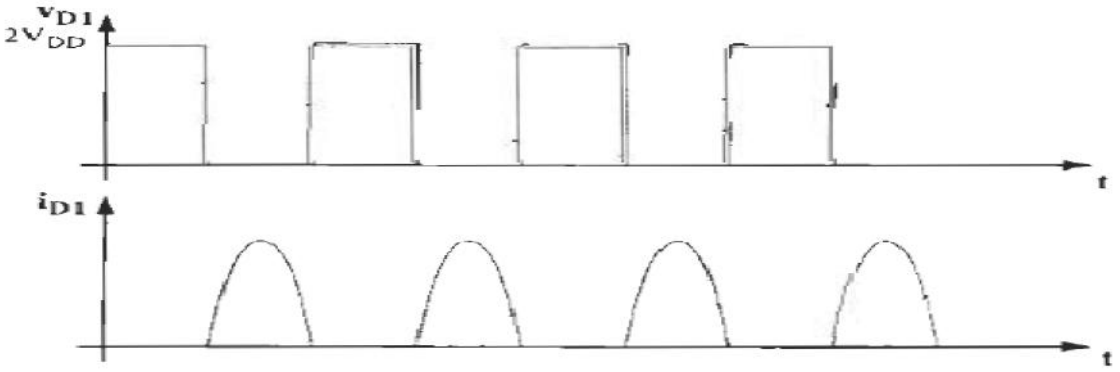


Fig 2. M1 drain voltage and current for ideal Class D amplifier.

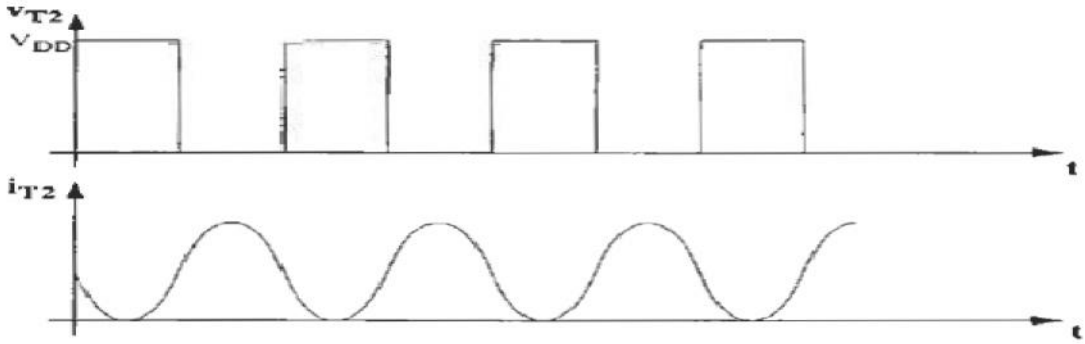


Fig 3. T2 secondary voltage and current for ideal Class D amplifier.

The normalized power handling of this amplifier happens to be

$$\frac{P_o}{v_{DS,\,on} \cdot i_{D,\,pk}} = \frac{1}{\pi} \approx 0.32, \qquad (1)$$

Which is better than a Class B push-pull and much better than a Class A amplifier. The Class D amplifier cannot normally provide linear modulation, but it does provide potentially high efficiency.

5. CLASS E AMPLIFIERS:- Class E topology as shown in Figure 4. the *BFL* simply provides a DC path to the supply and approximates an open circuit at RF. Note additionally that the capacitor C1 is conveniently positioned, for any device output capacitance can be absorbed into it.

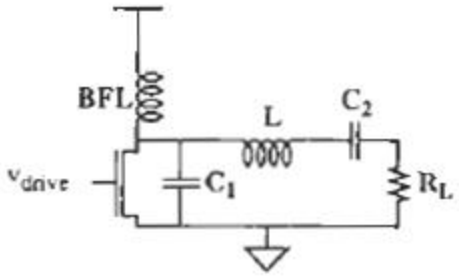


Fig 4.Class E amplifier

The design equations are as follows as given by

$$L = \frac{QR}{\omega},$$

$$C_1 = \frac{1}{\omega R(\pi^2/4 + 1)(\pi/2)} \approx \frac{1}{\omega(R \cdot 5.447)},$$

$$C_2 \approx C_1\left(\frac{5.447}{Q}\right)\left(1 + \frac{1.42}{Q - 2.08}\right).$$

(1)(2)(3)

For maximum efficiency, one desires the maximum *Q* consistent with the desired bandwidth. In practice, the achievable *Q* will often be substantially lower than the value that would limit bandwidth significantly. Once the *Q* is chosen, design of the Class E PA using the equations given.

Computation of drain current and voltage waveforms is difficult. However, they look something like the graphs in Figure 5 when everything is tuned tip. Note that the drain voltage has zero slope at turn-on, although the current is nearly n maximum when the switch turns off. Hence, switch dissipation can be significant during that transition if the switch isn't infinitely fast (as is the case with most switches you're likely to encounter). This dissipation can offset much of the improvement obtained by reducing the dissipation during the transition to the "on" state.

Fig 5. Waveforms for Class E amplifier.

Additionally note that each of the waveforms has a rather dramatic peak-to-average ratio. In fact a detailed analysis shows that the peak drain voltage is approximately *3.6VDD* while the peak drain current is roughly *1.7VDD/R.*

The maximum output power delivered to the load is

$$P_o = \frac{2}{1+\pi^2/4} \cdot \frac{V_{DD}^2}{R} \approx 0.577 \cdot \frac{V_{DD}^2}{R}.$$

The normalized power output capability is therefore

$$\frac{P_o}{v_{DS,on} \cdot i_{D,pk}} \approx 0.098. \qquad (4)(5)$$

Class E amplifiers do not scale gracefully with the trend toward lower-power (and hence lower-breakdown voltage) technologies. For these reasons, Class E amplifiers have not found wide application in CMOS form. However, discrete implementations do not suffer from the severe breakdown voltage constraints of deep-submicron CMOS, and consequently there are countless discrete Class E amplifiers with excellent performance.

6. CLASS F AMPLIFIERS:- Class F amplifier as shown in Figure1. Here, the output tank is tuned to resonance at the carrier frequency and is assumed to have a high enough *Q* to act as a short circuit at all frequencies outside of the desired bandwidth. The length of the transmission line is chosen to be precisely a quarter-wavelength at the carrier frequency. Recall that a quarter-wavelength piece of line has an "impedance reciprocation" property. That is, the input impedance of such a line is proportional to the reciprocal of the termination impedance:

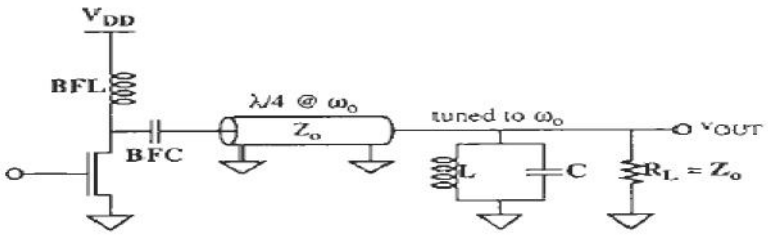


Fig 1. Class F amplifier.

$$Z_{\text{in}} = \frac{Z_o^2}{Z_L}.$$ (1)

We may deduce from this equation that a half-wavelength piece of line presents an input impedance equal to the load impedance, since two quarter-wave sections give us two reciprocations that undo each other.

At the carrier frequency, the drain sees a pure resistance of *RL= Z0* since the tank is an open circuit there, and the transmission line is therefore terminated in its characteristic impedance.

The high efficiencies possible are suggested by the waveforms depicted in Figure 2. The total peak-to-peak drain voltage is seen to be twice the supply voltage. Therefore, the peak-to-peak voltage of the fundamental component of *Vds* is

$$(4/\pi)2V_{DD}.$$ (2)

Note that the fundamental has a peak-to-peak value that actually exceeds the total *vos* swing, thanks to the magic of Fourier transforms. Now, since only the fundamental component survives to drive the load, the output power delivered is

$$P_o = \frac{[(4/\pi)V_{DD}]^2}{2R}.$$ (3)

Since the switch dissipates no power, we can conclude that the Class F amplifier is capable of 100% efficiency in principle. In practice, one can obtain efficiency superior to that of Class E amplifiers. Additionally, the Class F PA has substantially better normalized power-handling capability, since the maximum voltage is just twice the supply while the peak drain current is

$$i_{D,\text{pk}} = \frac{2V_{DD}}{R} \cdot \frac{4}{\pi} = \frac{8}{\pi} \cdot \frac{V_{DD}}{R}.$$

The normalized power handling capability is therefore

$$\frac{P_o}{v_{DS,\text{on}} \cdot i_{D,\text{pk}}} = \frac{\frac{[(4/\pi)V_{DD}]^2}{2R}}{2V_{DD} \cdot \left(\frac{8}{\pi} \cdot \frac{V_{DD}}{R}\right)} = \frac{1}{2\pi} \approx 0.16,$$ (4)(5)

or exactly half that of the Class D amplifier. In some respects, the Class F amplifier may be considered equivalent to a single-ended Class D amplifier. It should be emphasized that Class C, D, E, and F amplifiers are essentially *constant-envelope* amplifiers. That is, they do not normally provide an output that is proportional to the input and thus tend to perform best when all we ask of them is a constant-amplitude output.

6.1 INVERSE CLASS F (IF^{-1}):- The Class F amplifier's termination appears as an open circuit at odd harmonics of the carrier beyond the fundamental, and as a short circuit at even harmonics, the *illl'(,1'51' Class F* (often denoted by the shorthand F^{-1}) employs a termination that appears as an open circuit at even harmonics and as a short circuit at the odd harmonics as shown in Figure 1 below.

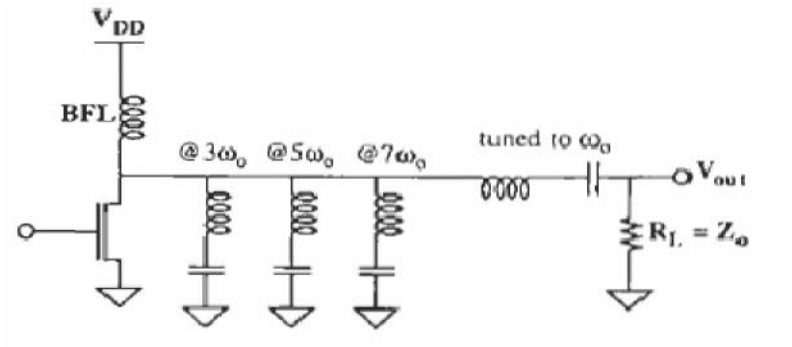


Fig 1. Inverse Class F amplifier (three-resonator lumped element example shown).

Again a transmission line may replace the lumped resonators when it is advantageous or otherwise practical to do so here a piece of line whose length is), λ/2 at the fundamental frequency replaces the paralleled series resonators and is interposed between the drain and the output series *LC* tank. For an infinite number of series resonators the drain voltage waveform consequently appears ideally as a (half) sinusoid and the current waveform as a square wave, as shown in Figure 2. Once again the lack of *V-I* overlap at the switching transitions accounts for the high theoretical efficiency of this architecture, just as with the Class E and standard Class F amplifiers.

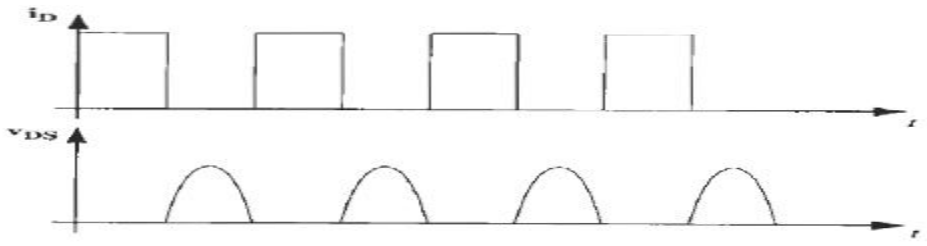


Fig 2. Drain voltage and current for ideal inverse Class F amplifier.

6.2 ALTERNATIVE CLASS F TOPOLOGY:- The topology of class F amplifier as shown in Figure 1 is elegant but the transmission line may be inconveniently long in many applications. Furthermore the benefits of infinite (or nearly infinite) impedance at odd harmonics other than the fundamental are somewhat undermined in practice by the transistor's own output capacitance. Hence A lumped approximation frequently performs nearly as well as the transmission-line version.

To create such a lumped approximation replaces the transmission line with a number of parallel resonant filters connected in series. Each of these resonators is tuned to a different odd harmonic of the carrier frequency. Quite often simply one tank tuned to *3wo* is sufficient. Significant improvement in efficiency is rarely noted beyond the use of the two tanks shown in Figure 15.15. For example use of one tank tuned to the third harmonic boosts the drain efficiency maximum to about 88%, compared to Class B's maximum of about 78%. Addition of tanks tuned to the fifth and seventh harmonics increases the Class F efficiency limit to 92% and 94%, respectively. Given that practical lank elements are not lossless, the law of diminishing returns rapidly makes the use of additional resonators worse than futile.

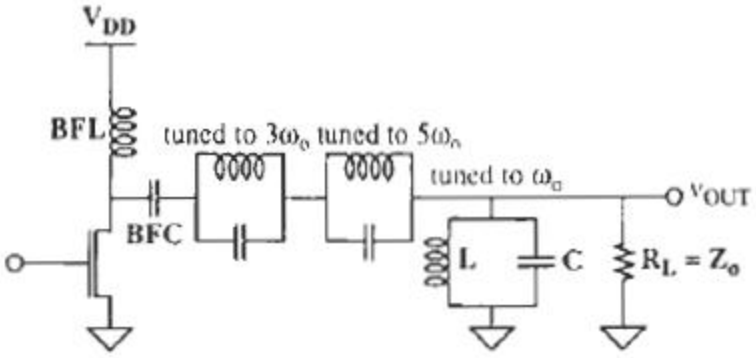


Fig 1.Alternative Class F amplifier.

7. LINEARIZED PLL MODELS:- The basic PLL architecture is shown in Figure 1, and is seen to consist of a phase detector and a voltage controlled oscillator (VCO). The phase detector compares the phase of an incoming reference signal with that of the VCO, and produces an output that is some function of the phase difference. The VCO simply generates a signal whose frequency is some function of the control voltage.

The general idea is that the output of the phase detector drives the VCO frequency in a direction that reduces the phase difference; that is, it's a negative feedback system**.**

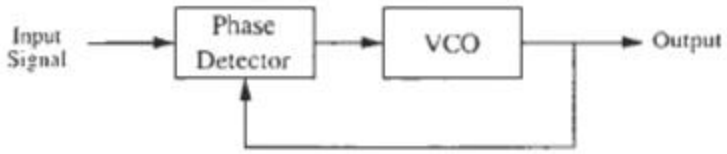


Fig 1. Phase-locked loop architecture.

Once the loop achieves lock, the phase of the input reference and VCO output signals ideally have a fixed phase relationship (most commonly 0° or 90°depending on the nature of the phase detector). Although both the phase detector and VCO may be highly nonlinear in practice it is customary to assume linearity when analyzing loops that have achieved lock.

Let us begin with a linearized PLL model. as shown in Figure 2. Because we are generally interested in the phase relationship between the input and output signals, the input and output variables are phases in this model, rather than the time waveforms of the actual inputs and outputs. Hence, if you are accustomed to thinking of signals as voltages in a block diagram, the input and output voltages are now proportional to phases.

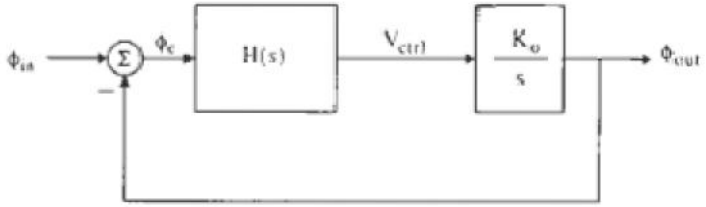


Fig2. Linearized PLL model.

Another consequence of choosing phase as the input-output variable is that the VCO, whose output frequency depends on a control voltage. is modeled as an integrator, since phase is the integral of frequency. The VCO gain constant *Ko* has units of radians per second per volt and merely describes what change in output frequency results from a specified change in control voltage. Also note that unlike ordinary amplifiers whose outputs are bounded, the VCO is a true integrator. The longer we wait, the more phase we accumulate (unless someone turns off the oscillator).

The phase detector is modeled as a simple subtracter that generates a phase error output ¢*c* that is the difference between the input and output phases. To accommodate gain scaling factors and the option of additional filtering in the loop, a block with transfer function *H(s)* is included in the model as well.

7.1. FIRST-ORDER PLL:- The simplest PLL is one in which the function *H(s)* is simply a scalar gain (call it *Kd.* with units of volts per radian). Because the loop transmission then possesses just a single pole, this type of loop is known as a first-order PLL. Aside from simplicity its main attribute is the ease with which large phase margins are obtained.

Offsetting those positive attributes is an important shortcoming, however: bandwidth and steady-state phase error are strongly coupled in this type of loop. Because one generally wants the steady-state phase error to bc zero, independent of bandwidth, first-order loops are infrequently used.

We may use our linear PLL model to evaluate quantitatively the limitations of a first-order loop. Specifically. the input-output phase transfer function is readily derived is

$$\frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{K_O K_D}{s + K_O K_D}. \qquad (1)$$

The closed-loop bandwidth is therefore

$$\omega_h = K_O K_D. \qquad (2)$$

To verify that the bandwidth and phase error are linked, let's now derive the input to error transfer function is

$$\frac{\phi_e(s)}{\phi_{in}(s)} = \frac{s}{s + K_O K_D}. \qquad (3)$$

If we assume that the input signal is a constant-frequency sinusoid of frequency *Wi,* then the phase ramps linearly with time at a rate of *Wi,* radians per second. Thus, the Laplace-domain representation of the input signal is

$$\phi_{in}(s) = \frac{\omega_i}{s^2},$$

so that

$$\phi_e(s) = \frac{\omega_i}{s(s + K_O K_D)}.$$

The steady-state error with a constant frequency input is therefore

$$\lim_{s \to 0} s\phi_e(s) = \frac{\omega_i}{K_O K_D} = \frac{\omega_i}{\omega_h}. \qquad (4)(5)(6)$$

The steady-state phase error is thus simply the ratio of the input frequency to the loop bandwidth; a one-radian phase error results when the loop bandwidth equals the input frequency. A small steady-state phase error therefore requires a large loop bandwidth.

In general a nonzero voltage is required to drive the VCO to the correct frequency. Since the control voltage derives from the output of the phase detector, there must be a nonzero phase error. To produce a given control voltage with a smaller phase error requires an increase in the gain that relates the control voltage to the phase detector output. Because an increase in gain raises the loop transmission uniformly at all frequencies, a bandwidth increase necessarily accompanies a reduction in phase error.

To produce zero phase error, we require an element that can generate an arbitrary VCO control voltage from a zero phase detector output implying the need for an infinite gain. To decouple the steady-state error from the bandwidth, however, this element needs to have infinite gain only at DC rather than at all frequencies. An integrator has the prescribed characteristics and its use leads to a second-order loop.

7.2. SECOND-ORDER PLL:- The model for a second-order PLL is shown in Figure1. The 90° negative phase shift contributed by the added integrator has to be offset by the positive phase shift of a loop-stabilizing zero. As with any other feedback system compensated in this manner the zero should be placed well below the crossover frequency to obtain acceptable phase margin.

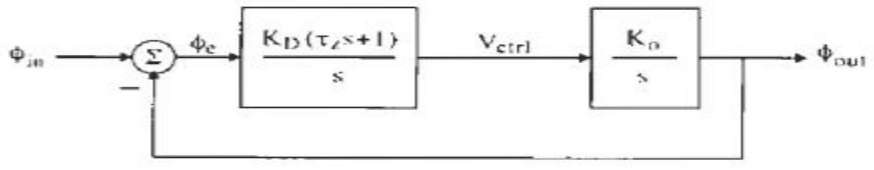


FIG 1. Model of second-order PLL

In this model, the constant *KD* has the units of volts per second because of the extra integration. Also thanks to the added integration the loop bandwidth may be adjusted independently of the steady-state phase error (which is zero here) as is clear from studying the loop transmission magnitude behavior graphed in Figure 2. The stability of this loop can be explored with the root-locus diagram of Figure 3. As the loop transmission magnitude increases (by increasing *KDKO)* the loop become progressively better damped because an increase in crossover frequency allows more of the zero's positive phase shift to offset the negative phase shift of the poles.

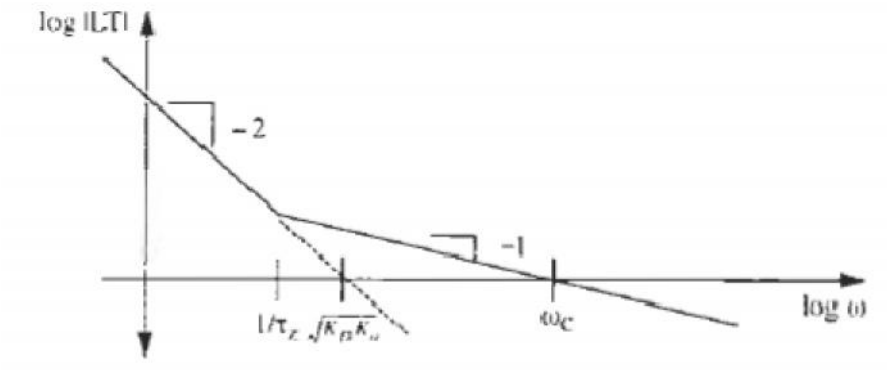


FIG 2. Loop transmission of second-order PLL

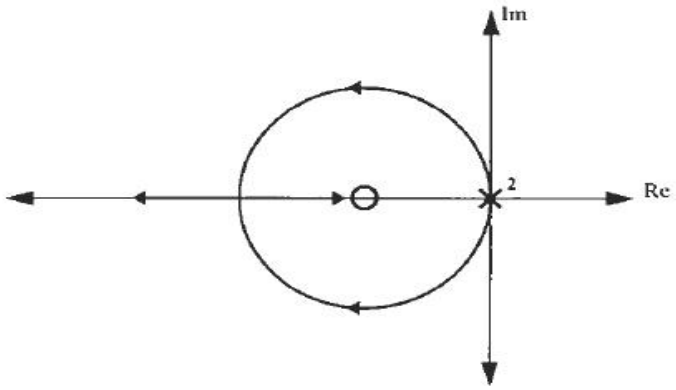


FIG 3. Root locus of second-order PLL.

For very large loop transmissions, one closed-loop pole ends up at nearly the frequency of the zero, while the other pole heads for infinitely large frequency. In this PLL implementation, the loop-stabilizing zero comes from the forward path, hence this zero also shows up in the closed-loop transfer function.

It is straightforward to show that the phase transfer function is

$$\frac{\phi_{out}}{\phi_{in}} = \frac{\tau_z s + 1}{(s^2/K_D K_O) + \tau_z s + 1},$$

from which we determine that

(1)

$$\omega_n = \sqrt{K_D K_O}$$

and

$$\zeta = \frac{\omega_n \tau_z}{2} = \frac{\tau_z \sqrt{K_D K_O}}{2}.$$

Furthermore, the crossover frequency for the loop may be expressed as

$$\omega_c = \left[\frac{\omega_n^4}{2\omega_z^2} + \omega_n^2 \sqrt{\frac{1}{4}\left(\frac{\omega_n}{\omega_z}\right)^4 + 1} \right]^{1/2},$$

(2)(3)(4)

which simplifies considerably if the crossover frequency is well above the zero frequency, as it often is

$$\omega_c \approx \frac{\omega_n^2}{\omega_z}.$$

(5)

Both Figure 2 and Eqn. 4show that the crossover frequency always exceeds *wn* which from Figure 2 and Eqn.2 is the extrapolated crossover frequency of the loop with no zero. Finally it should be clear that increasing the zero's time constant improves the damping, given a fixed *wn.* Thus, the bandwidth and stability of a second-order loop may be adjusted as desired while preserving a zero steady-state phase error.

JITTER PEALKINGIN SECOND-ORDER PLLS:- From the root locus for this loop, we see that the zero is to the right of its associated (closed-loop) pole at larger damping ratios. Hence the closed-loop frequency response initially exceeds unity until the zero's effect is cancelled by the poles (see Figure 1).

We see that there is a rise with frequency starting at the zero location then a flattening caused by the first pole. As seen in the figure the phase transfer function has a magnitude greater than unity above the zero frequency until the second pole introduces a sufficient rolloff. There is thus a band of frequencies bounded roughly by the zero location and the second pole where the magnitude of the transfer function exceeds unity.

The implication of this peaking is that if there is any modulation (intended or otherwise) on the input with spectral components within that certain frequency band, the output modulation will have a phase excursion that exceeds the excursion on the input. Unfortunately, we can see from the locus that such peaking is an inherent property of such loops as long as the zero is contributed by the forward path. Therefore if this peaking is to be kept to a minimum we require large loop transmissions to keep the first pole as close to the zero as possible." Although this jitter peaking may be totally eliminated by using a voltage-controlled delay element to provide the loop zero in the feedback path. it is satisfactory in most RF applications simply to choose sufficiently large damping ratios.

8. PHASE DETECTORS:- We now consider a few implementation details to see how real PLLs are built and how they behave.

8.1 THE ANALOG MULTIPLIER AS A PHASE DETECTOR: - In PLLs that have sine-wave inputs and sine-wave VCOs, the most common phase detector by far is the multiplier, often implemented with a Gilbert-type topology. For an ideal multiplier it isn't too difficult to derive the input-output relationship, as shown in Figure 1.

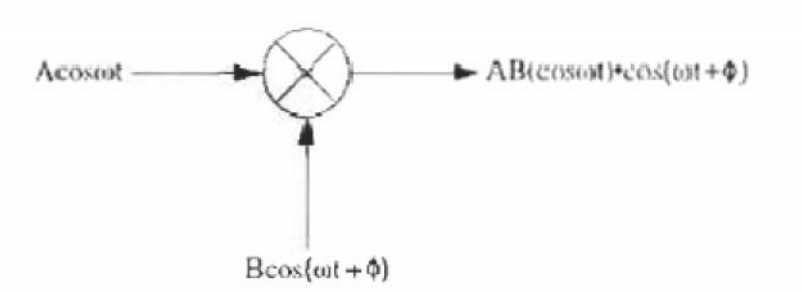


Fig 1. Multiplier as phase detector

Using some trigonometric identities, we find that the output of the multiplier may be expressed as

$$AB\cos\omega t\cos(\omega t+\phi)=\frac{AB}{2}[\cos(\phi)-\cos(2\omega t+\phi)]. \tag{1}$$

Note that the output of the multiplier consists of a DC term and a double-frequency term. For phase detector operation, we are interested only in the DC term. Hence, the average output of the phase detector is

$$\langle AB\cos\omega t\cos(\omega t+\phi)\rangle=\frac{AB}{2}[\cos\phi]. \tag{2}$$

We see that the phase detector gain "constant" is a function of the phase angle and is given by

$$K_D = \frac{d}{d\phi}\langle V_{out}\rangle = -\frac{AB}{2}[\sin(\phi)]. \tag{3}$$

If we plot the average output as a function of phase angle. we get something that looks roughly as shown in Figure2. Notice that the output is periodic. Further note that the phase detector gain constant is zero when the phase difference is zero, and is greatest when the input phase difference is 90°. Hence, to maximize the useful phase detection range the loop should be arranged to lock to a phase difference of 900• For this reason, a multiplier is often called a *quadrature* phase detector.

When the loop is locked in quadrature, the phase detector has an incremental gain constant given by

$$K_D\big|_{\phi=\pi/2} = \frac{d}{d\phi}\langle V_{out}\rangle\Big|_{\phi=\pi/2} = -\frac{AB}{2}. \tag{4}$$

we will glibly ignore minus signs. The reason for this neglect is that a loop may servo to either a 90^0 or -90^0 phase difference (but not to both), depending on the net number of inversions provided by the rest of the loop elements. Because there are two phase angles (within any given 2pi interval) that result in a zero output from the phase detector, there would seem to be two equilibrium points to which the loop could lock. However, one of these points is a stable equilibrium, whereas the other is a *metastable* point from which the loop must eventually diverge.

That is, only one of these lock points corresponds to negative feedback. When speaking of phase errors for a quadrature loop, we calculate the departure from the equilibrium condition of a 90^0 phase difference. Thus, although the phase difference is 90° in an ideal quadrature loop, the phase *error* is considered to be zero.

8.1 THECOMMUTATING MULTIPLIER AS A PHASE DETECTOR:-

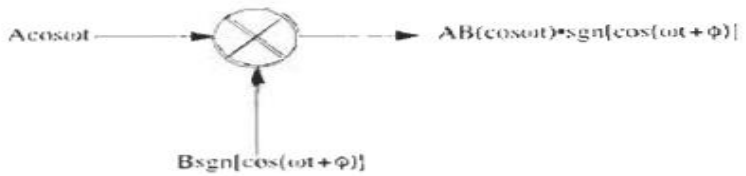


Fig1. Multiplier with one square-wave input .

$$\text{sgn}(x) = 1 \quad \text{if } x > 0,$$
$$\text{sgn}(x) = -1 \quad \text{if } x < 0.$$

(1)(2)

Now, recall that a square wave of amplitude *B* has a fundamental component whose amplitude is *4B/Pi,* If we assume that we care about only the fundamental component of the square wave, then the average output of the multiplier is

$$\langle V_{\text{out}} \rangle = \frac{4}{\pi}\frac{AB}{2}[\cos(\phi)] = \frac{2}{\pi}AB[\cos(\phi)].$$

(3)

The corresponding phase detector gain is similarly just *4/Pi* times as large as in the purely sinusoidal case is

$$K_D\big|_{\phi=\pi/2} = \frac{d}{d\phi}\langle V_{\text{out}} \rangle\Big|_{\phi=\pi/2} = -\frac{2AB}{\pi}.$$

(4)

Although the expressions for the phase detector output and gain are quite similar to those for the purely sinusoidal case, there is an important qualitative difference between these two detectors. Because the square wave consists of more than just the fundamental component, the loop can actually lock onto harmonics or sub harmonics of the input frequency. Consider, for example, the case where the B square-wave square waves!' consist of odd harmonics, and the third harmonic will then be at the same frequency as the input sine wave. Those two signals will provide a DC output from the multiplier.

Because the spectrum of a square wave drops off as I*f,*14 the average output gets progressively smaller as we attempt to lock to higher and higher harmonics. The attendant reduction in phase detector gain constant thus makes it more difficult to achieve or maintain lock at the higher harmonics, but this issue must be addressed in all practical loops that use this type of detector. Sometimes harmonic locking is desirable, and sometimes it isn't If it isn't, then the VCO frequency range usually has to be restricted (or acquisition carefully managed) in order to prevent harmonic locking.

8.3 THE EXCLUSIVE·OR GATE AS A PHASE DETECTOR :- If we now drive an analog multiplier with square waves on *both* inputs, we could analyze the situation by using the Fourier series for each of the inputs, multiplying them together and so forth.

In this case, the two square-wave inputs produce the output shown in Figure 1.As we change the input phase difference the output takes the form of a square wave of varying duty cycle, with a 50% duty cycle corresponding to a quadrature relationship between the inputs. Since the duty cycle is in fact proportional to the input phase difference, we can readily produce a plot (Figure 2) of the average output as a function of the input phase difference.

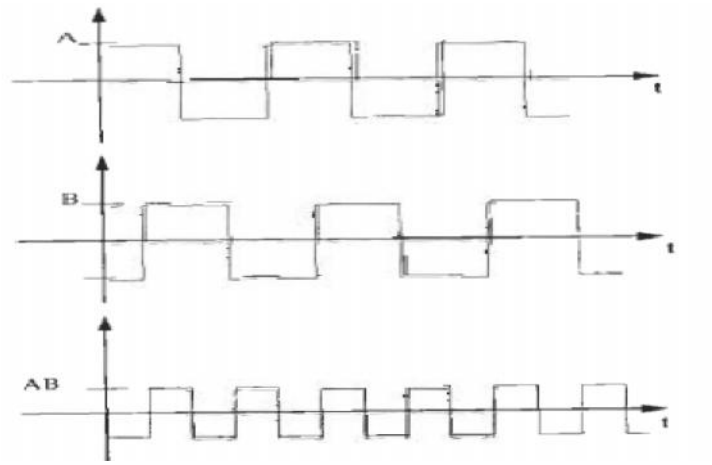


Fig 1. Multiplier inputs *and* output

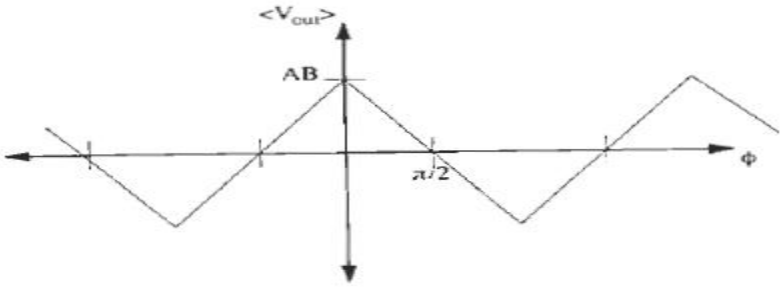


Fig 2. Multiplier characteristic with two square-wove inputs

The phase detector constant *is* a constant in this instance, and is equal to

$$K_D = \frac{2}{\pi} AB. \qquad (1)$$

We see that, within a scale factor, this phase detector has the same essential behavior as an analog multiplier with sinusoidal inputs, again interpreting phase errors relative to quadrature. As in the case with one square-wave input this phase detector allows the loop to lock to various harmonics of the input.

If we examine the waveforms for this detector more closely we see that they have precisely the same shape as would be obtained from using a digital exclusive-OR gate, the only difference being DC offsets on the inputs and outputs. as well as an inversion here or there. Hence, an XOR may be considered an overdriven analog multiplier. For the special case where the inputs and output are logic levels that swing between ground and some supply voltage *VDD* (as in CMOS), the phase detector output has an average value that behaves as graphed in Figure 3.

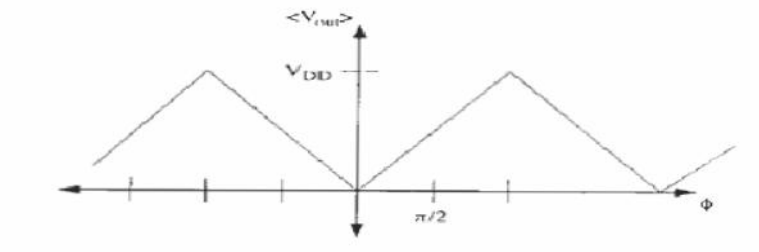


Fig3 . Characteristic of XOR as quadrature phase detector.

The corresponding phase detector gain is then

$$K_D = \frac{V_{DD}}{\pi}. \qquad (3)$$

Because of the ease with which they are implemented, and because of their compatibility with other digital circuitry, XOR phase detectors are frequently found in simple IC PLLs.

9. LOOP FILTERS AND CHARGE PUMPS:- We now consider how to implement the rest of the loop. We'll take a look at various types of loop filters and survey a couple of common techniques for realizing VCOs. We'll wrap up by going through an actual example to illustrate a typical design procedure.

9.1 LOOP FILTERS:- Recall that we generally want to have zero phase error in lock. Now the VCO requires some control voltage to produce an output of the desired frequency. To provide this control voltage with a zero output from the phase detector (and hence zero phase error) the loop filter must provide integration. Their to ensure loop stability, the loop filter must also provide a zero.

A classic architecture that satisfies these requirements appears as Figure 1. It should be easy to deduce the general properties of the loop filter without resorting to equations.

At very low frequencies the capacitor's impedance dominates the op-amp's feedback so the loop filter behaves as an integrator. As the frequency increases, though the capacitive reactance decreases and eventually equals

the series resistance *R2*. Beyond that frequency the capacitive reactance becomes increasingly negligible compared with *R2* and the gain ultimately flattens out to simply *-R2/R1*.

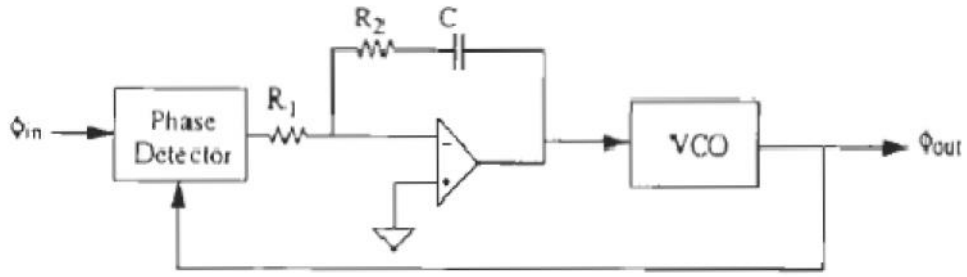


Fig 1. PLL with typical loop filter

Stating these observations another way, we have a pole at the origin and a zero whose time constant is *R2C*, Furthermore, the value of R1 can be adjusted to provide whatever loop transmission magnitude we'd like, so the op-amp circuit provides us with the desired loop filter transfer function.

Before going further, it should be mentioned that PLLs need not include an active loop filter of the type shown. In the simple's case, a passive *RC* network could be used to connect the phase detector with the VCO, However the static phase error will then not be zero, and the loop bandwidth will be coupled (inversely) with the static phase error. Because of these limitations, such a simple loop filter is used only in noncritical applications.

The circuit of the figure is commonly used in discrete implementations, but a different (although functionally equivalent) approach is used in most ICs. The reason is that it is not necessary to build an entire op-amp to obtain the desired loop filter transfer function. A considerable reduction in complexity and area (not to mention power consumption) can be obtained by using an element that is less general-purpose than an op-amp.

A popular alternative to the op-amp loop filter is the use of a *charge pump* working in tandem with an *RC* network. Here, the phase detector controls one or more current sources and the *RC* network provides the necessary loop dynamics.

Figure 2 shows how a charge pump provides the necessary loop filter action. Here the phase detector is assumed to provide a digital "pump up" or "pump down" signal. If the phase detector determines that the VCO output is lagging the input reference. it activates the top current source, depositing charge onto the capacitor

(pumping up). If the VCO is ahead, the bottom current source is activated, withdrawing charge from the capacitor (pumping down)

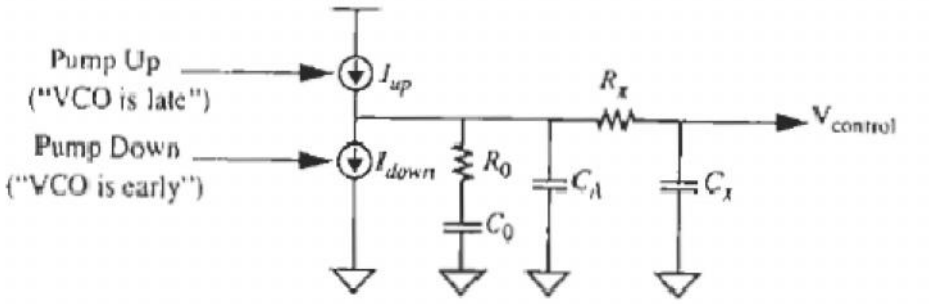


FIG 2. Idealized PLL charge pump with third order loop filter

If there were no resistor *Ro* then we would have a pure integration. As usual, the series resistor provides the necessary loop-stabilizing zero by forcing the high frequency asymptotic impedance to a nonzero value. Elements *CA,R*x. and Cx provide additional filtering.

When that detector is used with the charge pump of Figure 2 the net pump current is given by

$$I = I_{\text{pump}} \frac{\Delta\phi}{2\pi}, \tag{1}$$

where $I_{\text{pump}} = I_{\text{up}} = I_{\text{down}}$. This current, multiplied by the impedance of the filter network connected to the current sources, gives the output voltage.

A typical charge pump appears in Figure 3. Analysis of this circuit highlights some of the more important design considerations associated with charge pump design .Transistors *M1* through *M4* are differential switches operated by the up and down commands from the phase detector. Depending on the state of those commands

either source current I_{up} or sink current I_{down} is steered to the output node O_p. Thus,. I_{out} equals I_{up} or I_{down}, depending on the phase detector state.

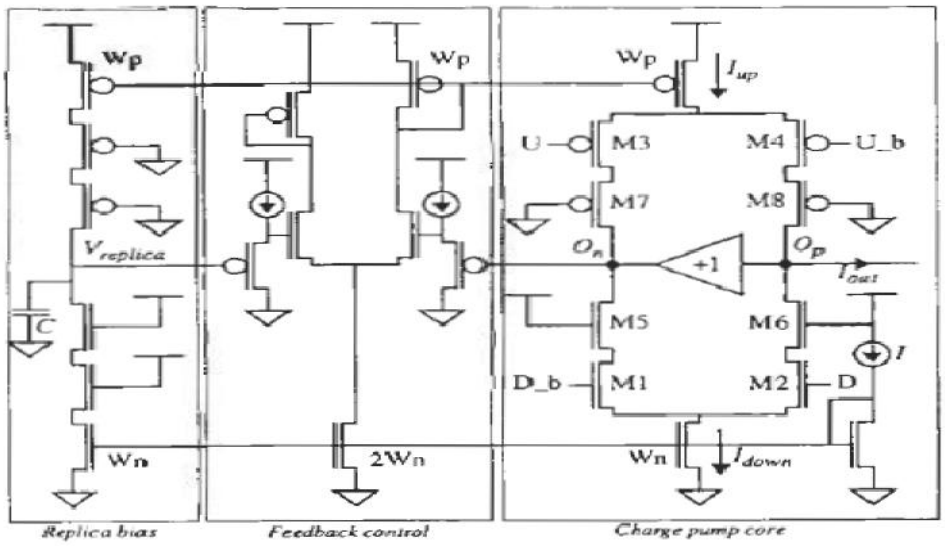


Fig 3. Example of PLL charge pump.

The switches are cascoded by transistors *M5* to *M8* for high output impedance because any leakage increases spur power. To understand why, consider the locked condition. With low leakage, very little net charge needs to be delivered by the charge pump per cycle. There is thus very little ripple on the control line and hence very little modulation of the VCO. As leakage increases, however, the charge pump must make up for an increasing amount of lost charge implying the necessity for an increasing static phase error.

Control-Line Ripple and Higher-Order Poles:

LOOP FILTER DESIGN:

Step 1. ***Specify a phase margin*** **once this value is chosen. it sets a constraint on capacitor values specifically.**

$$\mathrm{PM} \approx \operatorname{atan}\left(\sqrt{b+1}\right) - \operatorname{atan}\left(\frac{1}{\sqrt{b+1}}\right). \quad \textbf{(1)}$$

where "atan" is shorthand for "arctangent" and

$$b = \frac{C_0}{C_A + C_X}. \quad \textbf{(2)}$$

It's probably prudent to choose a phase margin a few degrees above the target value to absorb the inevitable negative phase contributions by the sampled nature of the loop and by unmodeled poles and other destabilizing sources. For example suppose the specified phase margin target is 45^0. If we therefore design for 50°, we find (through iteration, for example) that *b* should be about 6.5.

Step2. *Select loop crossover frequency,* based on specifications on tracking bandwidth, for example. Combined with the results of Step 1 we find the location of the loop stabilizing zero as follows.

We know that maximizing the loop bandwidth maximizes the frequency range over which the presumably superior phase noise characteristics of the reference oscillator are conferred on the output. Unfortunately, the loop is a sampled data system we can only push up the crossover frequency to about a tenth of the phase comparison frequency before the phase lag inherent in a discrete-time phase detector starts to degrade phase margin seriously. As a specific example assume that the reference frequency (and hence phase comparison frequency) is 2 MHz. Choosing a crossover frequency of 100 kHz i~ more than a decade below the reference frequency, so let's use that value in what follows (you arc free 10 choose some other value, within limits).
For the crossover frequency we have

$$\omega_c \approx \frac{\sqrt{b+1}}{\tau_z} = \frac{\sqrt{b+1}}{R_0 C_0}. \qquad (3)$$

Step 3. *Calculate* Co. the value of the zero-making capacitor, thus

$$C_0 = \frac{I_P}{2\pi}\frac{K_0}{N}\frac{b}{\sqrt{b+1}}\frac{1}{\omega_c^2}, \qquad \textbf{(4)}$$

where *Ip* is the charge pump current, *N* is the divide modulus, and *K0* is the VCO gain constant in radians per second per volt.

Step 4. *Calculate Ro = τxCo.* This completes the design of the main part of the loop filter.

Step 5. *Select τx= RxCx* within the following range is

$$0.01 < \tau_x/\tau_z < 0.1. \qquad \textbf{(5)}$$

Within these wide limits is considerable freedom of choice. You can choose to design for the arithmetic mean. or the geometric mean. or some other kind of mean. Typically one selects *τx* to be 1/30 to *1/20* of *τx* .A bigger time constant results in somewhat better filtering action but tends to be associated with lower stability. Since loop constants aren't constant. it is prudent to design for *some* margin.

Step 6. Complete the remaining calculations

Back in Step 1 we developed a constraint on the capacitance ratios. Having found one of the capacitances, we now know the sum of CA and C*x* . You are free to select the individual values over a quite wide range, as long as they sum to the correct value. Arbitrarily setting them equal is a common choice." Having done so then allows us to determine their absolute values, which subsequently allows us to determine the value of *Rx.*

9.2.VCOs:- We examine here one common architecture for realizing VCOs in integrated circuits the current-starved ring oscillator. in which the effective propagation delay of each inverter in the ring is controlled by a current source.

RING OSCILLATORS:- Ring oscillators are an extremely popular idiom, since they derive from digital-like building blocks. We'll see later that, compared to tuned oscillators (i.e.. those that explicitly use high- *Q* resonators) they have substantially inferior phase noise performance for a given level of power consumption. For many applications, however, their relatively large tuning range and simplicity are strong enough attributes to make them attractive.

The controllable ring oscillator derives from the uncontrolled ring oscillator and consists simply of *n* inverters in a ring, where *n* is odd.In its simplest form, it appears as shown in Figure 1.

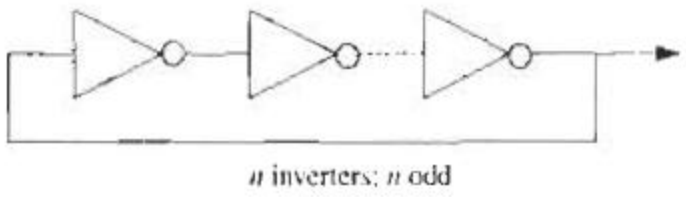


Fig 1 ring oscillator.

In the simplest analysis of such an oscillator, it is assumed that each inverter can be characterized by a propagation delay *T*pd. No stable DC point exists, and a logic level propagates around the loop, experiencing one net inversion each traversal. The oscillation period is therefore simply twice the total propagation delay is

$$f_{osc} = \frac{1}{2n \cdot T_{pd}}. \qquad (2)$$

Now, to convert this thing into a controllable oscillator, the propagation delay seems the most natural quantity to adjust.

One can imagine a great many specific methods for adjusting the delay, but they all boil down 10 either changing the load (e.g., by varying the effective amount of capacitance seen by each inverter output) or

varying the current drive of the inverters .One cheesy way to accomplish the latter is shown in Figure 2, where a PMOS current mirror provides a limited, variable pull-up current to the CMOS inverter." By adjusting this current, the effective propagation delay of the inverter can be adjusted, altering the oscillation frequency in the process.

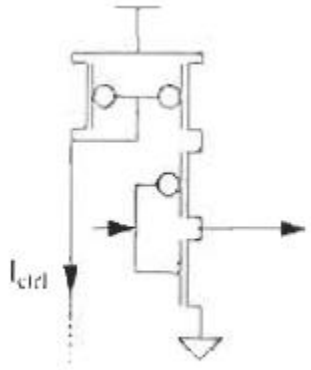


Fig 2. Sirnple current-starved CMOS inverter.

The ring oscillator (and its many variants) requires only elements that are normally available in ordinary digital process technology. This attribute, combined with its fundamental simplicity, has made the ring oscillator a near-ubiquitous topology in ICs.