UNIT - 1

1.1) Introduction to VLSI Technology:

Introduction to IC Technology

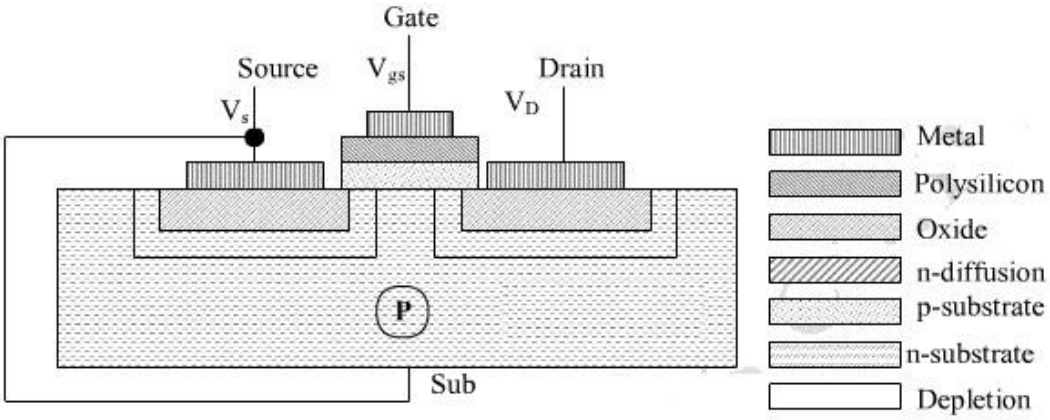
Electronics, and in particular the integrated circuit has made possible the design of powerful and flexible proceesors which provide highly intelligent and adaptable devices for the user. Integrated circuit memories have provided the essential elements to complement these proceesors and, together with a wide range of Logic and analog integrated circuitry, they have provided the system designer with components of considerable capability and extensive application.

Invention of transistor was followed by the development of the integrated circuit (IC). Over the past several years, silicon CMOS technology has become the dominant fabrication process for relatively high performance and cost effective VLSI Circuits. The revolutionary nature of this development is indicated by the way in which the number of transistors integrated in circuits on a single chip has grown as indicated in the graph below:

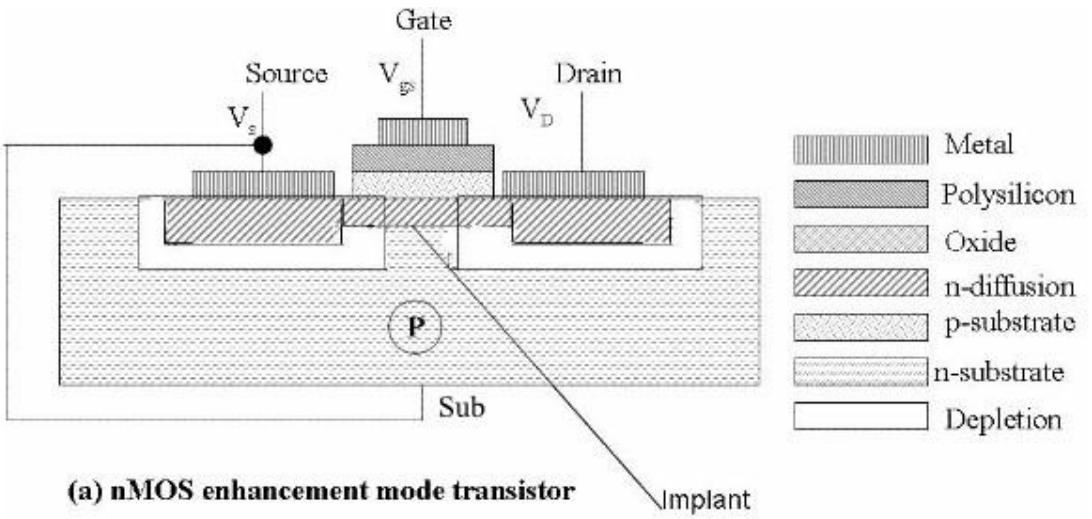
1.2) operation of MOS,PMOS,NMOS transistors

BASIC MOS TRANSISTORS

MOS means Metal oxide semiconductor technology. The basic n MOS enhancement and depletion mode transistors are shown in the figures below.



(a) nMOS enhancement mode



(a) nMOS enhancement mode transistor

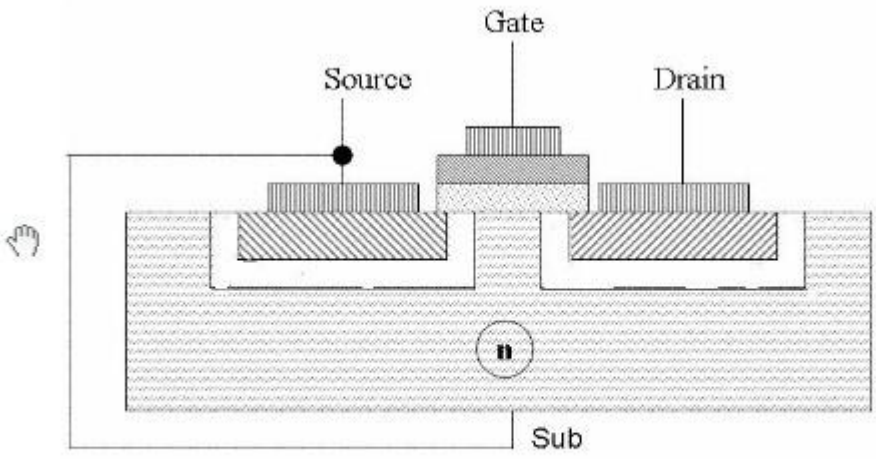
n MOS devices are formed in a P-type substrate of moderate doping level. The source and drain regions are formed by diffusing n – type impurities through suitable marks into these areas to give the desired n – impurity concentration and give rise to depletion regions which extend mainly in the more lightly doped P region as shown Thus, source and drain are isolated from one another by two diodes. Connections to the Source and drain are made by a deposited metal layer.

Consider the enhancement mode device first. A Polysilicon gate is deposited on a layer of insulation over the region between source and drain. The basic enhancement mode is shown in the figure (a) in which the channel is not established and the device is in a non-conducting condition,

$V_D = v_S = V_{ge} = 0$. If this gate is connected to suitable positive voltage with respect to the source, then the electric field established between the g and the substrate gives rise to a charge inversion region in the substrate under the gate insulation and a conducting path or channel is formed between source and drain.

The channel may also be established so that it is present under the condition $V_{gs} = O$ by implanting suitable impurities in the region between source and drain during manufacture. This is the n MOS depletion mode transistor. The source and drain are connected by a conducting channel, but the channel may now be closed by applying a suitable negative voltage to the gate.

In both cases, variations of the gate voltage allow control of any current flow between source and drain.



(c) pMOS enhancement mode transistor

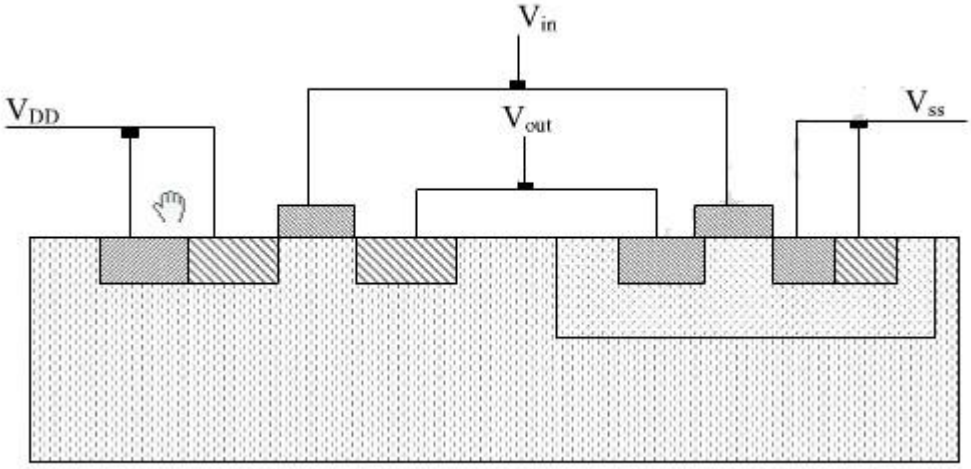
Figure 1.4 MOS transistors (V_D=0V. Source gate and substrate to 0 V)

The above figure shows the PMOS transistor structure for an enhancement mode device. In this case, the substrate is of n – type material and the source and drain diffusions are consequently P- type. In the figure, the conditions are for an unbiased device, however the application of negative voltage of suitable magnitude $(|V_t|)$ between gate and source will give rise to the formation of a channel (P-type) between the source and drain and current may then flow if the drain is made negative with respect to the source. In this case current is carried by the holes as opposed to electrons. PMOS transistors are slower than n MOS since whole mobility up is lees than electron mobility μ_n.

CMOS

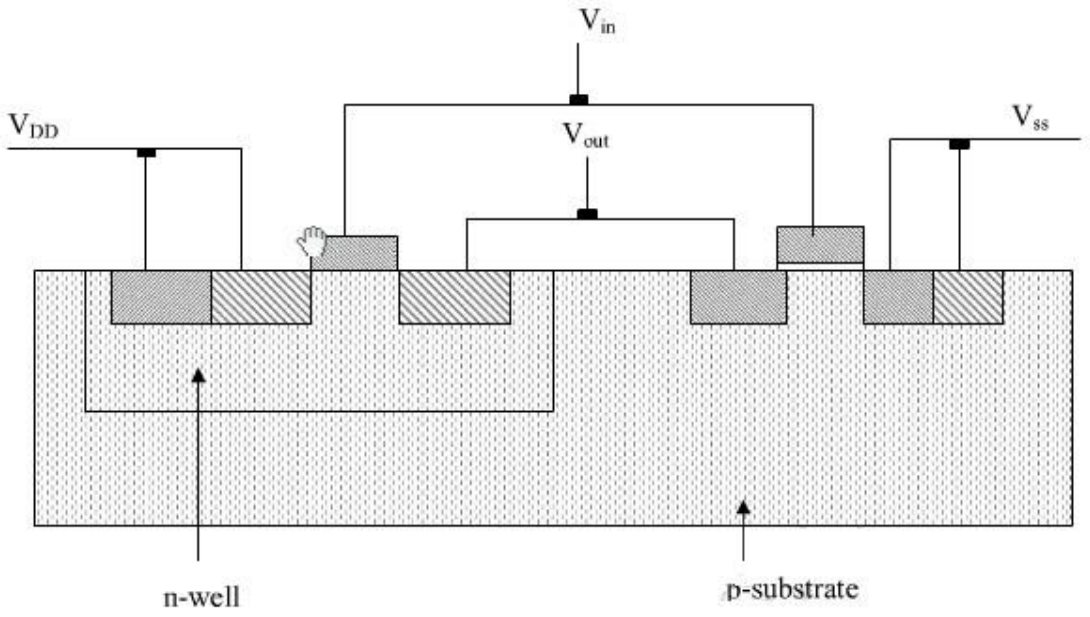
There are two types of fabrication of CMOS basically. P – well and n – well inverters are the major ones.

In CMOS P- well inverter, the structure consist of an n – type substrate in which P- devices may be formed by suitable marking and diffusion and, in order to accommodate n – type devices, a deep P – well is diffused into the n – type substrate.



CMOS p-well inverter showing V_{DD} and V_{SS} substrate

N – well CMOS circuits are superior to P-well because of the lower substrate bias effects on transistor threshold voltage and inherently lover Parasitic capacitances associated with source and drain regions. The CMOS n – well inverter is shown in figure below.



Cross-sectional view of n well CMOS

1.3) Fabrication of CMOS inverter

Basic CMOS Technology

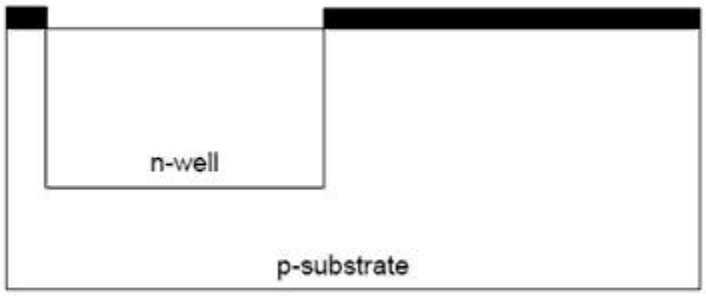
In early days of technology, the control gate of the MOS transistor was made with aluminum instead of polycrystalline silicon. It was difficult to align the metal over the channel precisely; an offset in one direction or other would create a non-functioning of the transistor. To overcome these problems, the poly-silicon gate was introduced. This polysilicon would be deposited before source/drain diffusion. During the diffusion, source and drain regions are self-aligned with respect to the gate. This self-alignment structure reduces the device size. In addition, it eliminates the large overlap capacitance between gate and drain, while maintaining a continuous inversion layer between source and drain. In the case of metal gate process, Al deposition has to be carried out almost at the end of fabrication because further high temperature processing would melt Al. In case of self-aligned poly silicon gate technology, these restrictions are also circumvented.

Basic n-well CMOS process

In a standard n-well process, one of the first things made is the n-well in a p type substrate. Once the n-well is created, the active areas can be defined. The MOSFET is build within this active area. A very thin layer of silicon dioxide is grown on the surface. This will be used to insulate the gate from the surface. The thin layer of SiO_2 is grown and covered with Si_3N_4. This will act as a mask during the subsequent channel stop implant and field oxide growth. The channel stop implant is to prevent conduction between unrelated transistor source/drains. A thick additional layer oxide grows in both directions vertically where Si_3N_4 is absent. Layer of silicon dioxide under the polysilicon gate (which will be created later) is known as gate oxide and that is not directly under the gate of a transistor is known as field oxide. The field oxide provides isolation between transistors. A threshold adjustment implant would be the next process step. This is carried out to balance off the threshold voltage differences. The P-MOS results in a higher

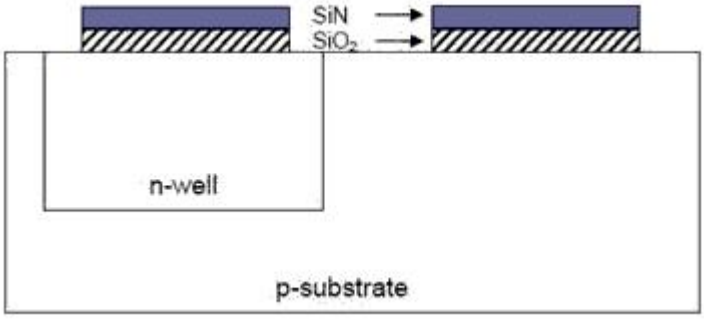
threshold voltage level than nMOS with normal doping concentrations. With additional negative charges buried inside the channel, V_T for pMOS could be controlled.

(a)



Formation of n-well

(b)

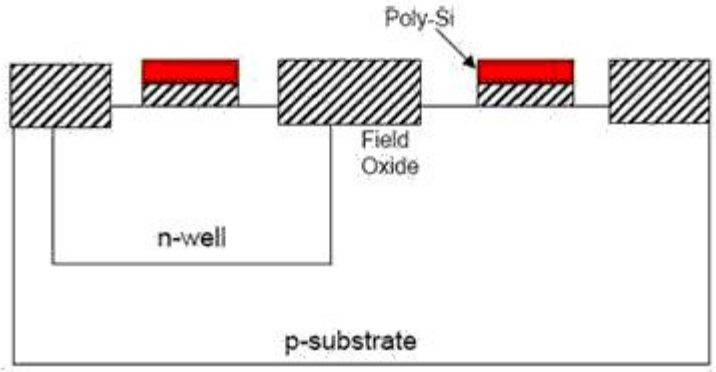


Gate oxide covered with silicon nitride in the active areas

Polysilicon deposition is carried out and gate definition is then completed using the mask shown in fig (c). Note that the connection between two gate inputs in a CMOS inverter is achieved using the poly silicon. The source and drain diffusions for pMOS is carried out using p-type diffusion. Boron is the most popular element used for this step. Similarly, source and drain diffusions for nMOS is carried out using n-type diffusion. Phosphorous and Arsenic can both be used for this step. Additional oxide is created, and then the contact holes are cut in the oxide down to the diffusions and polysilicon. These contacts can be filled by metal permitted to flow into the holes. The drains of pMOS and nMOS transistors are connected by a metal line in order to take the output from the CMOS inverter.

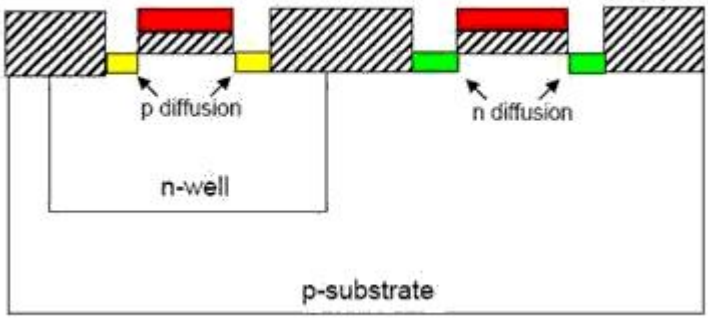
Top view of Poly silicon mask

(d)



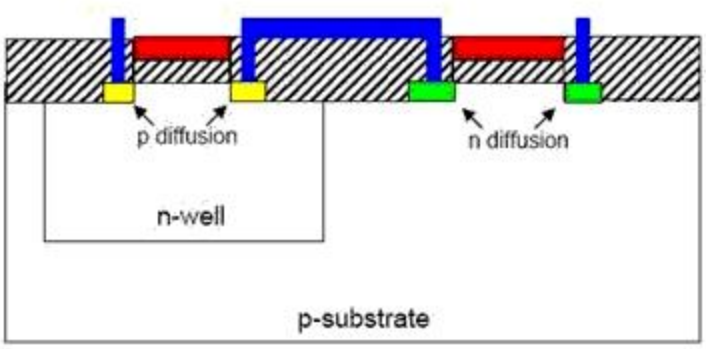
Poly silicon gate definition is completed

(e)



Transistor source/drain diffusion is completed

(f)



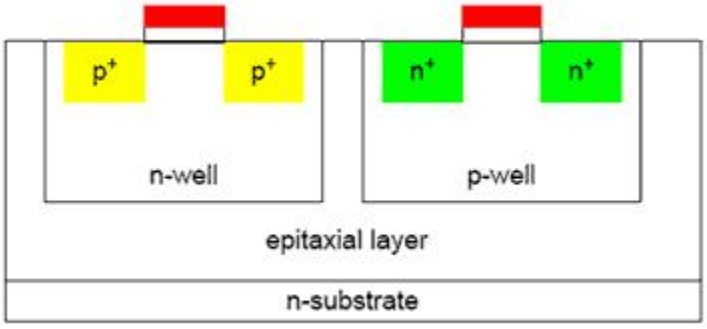
Cross section of a CMOS inverter in an n-well process

P-well process

Prior to the n-well process p-well process was popular. P-well process is preferred in circumstances where balanced characteristics of the nMOS and pMOS are needed. It has been observed that the transistors in the native substrate tend to have better characteristics than that was made in a well. Because p devices inherently have lower gain than devices, n well process amplifies this difference while a p-well process moderates the difference. The standard p-well process steps are is similar to n-well process, except that a p-well is implanted instead of an n-well as a first step. Once the p-well is created, the active areas and subsequently poly gates can be defined. Later diffusions can be carried out to create source and drain regions. Finally, metal is deposited and patterned for contacts.

Twin-Tub process

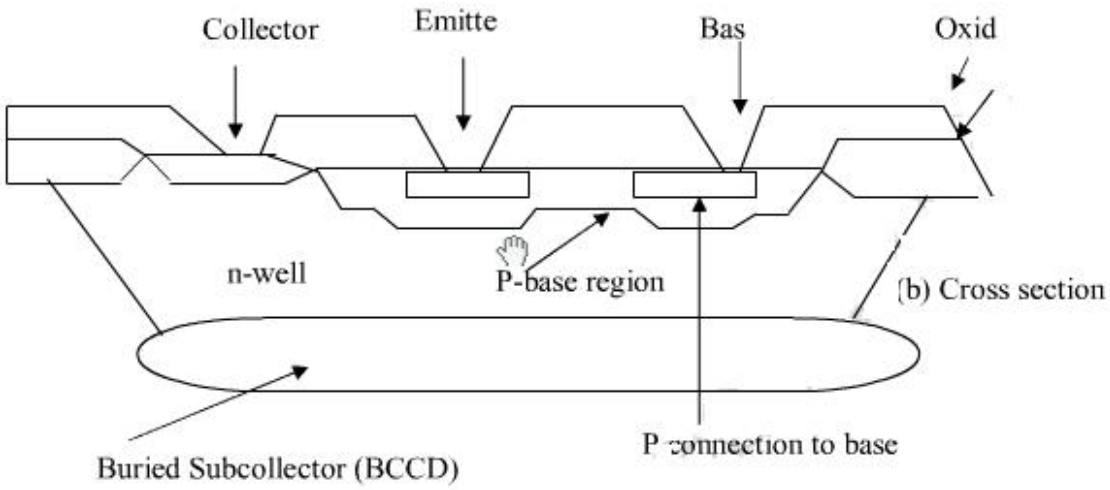
It is also possible to create both a p-well and an n-well for the n-MOSFET's and p-MOSFET respectively in the twin well or twin tub technology. Such a choice means that the process is independent of the dopant type of the starting substrate (provided it is only lightly doped).



A simplified sketch of twin-well CMOS process cross section

BICMOS TECHNOLOGY

The limited drive capabilities of MOS transistors can be overcome with the BiCMOS npn transistor consists of a P^+ base region, n^+ collector area and the buried sub collector (BCCD)



Arrangement of BICMOS npn transistor

OXIDATION

Oxidation refers to the chemical process of reaction of S i with 0_2 to form SiO_2

There are different types of oxidation such as

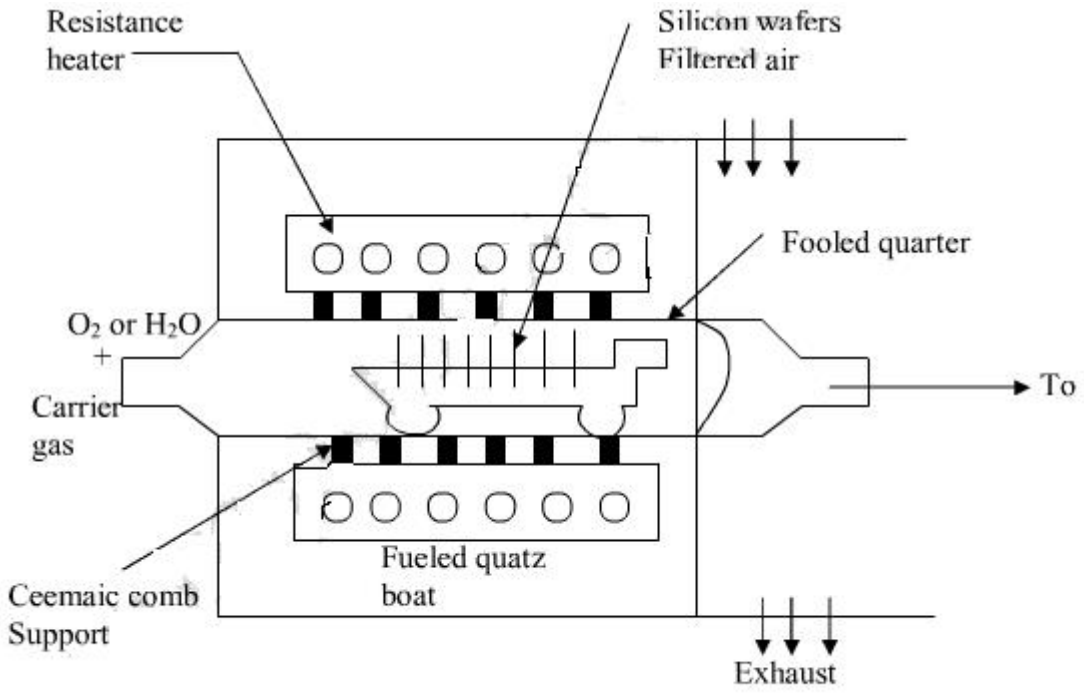
(i) Thermal oxidation

(ii) High presses are oxidation.

(iii) Plasma oxidation

Thermal oxidation:

Thermal oxidation has been a principal technique in silicon IC technology. Schematic croes – section of a resistance heated oxidation furnace is shown below:



Resistance heated oxidation furnace

The reactor for thermal oxidation consists of resistance heated finance a cylindrical fused quartz tube and a source of pure day oxygen or water vapour. The loading end of the furnace tube antes into a vertical flow hood where a flow of filtered air us maintained. This reduces dust and particulate matter in the air surrounding the wafers and thus protects the wafers from contamination at the time of loading.

A cylindrical fused quartz tube contains the Wafers which are held vertically in a slotted quartz boat and are expored source of oxygen

The Chemical equations for oxidation of silicon are

$S\,i\,(S) + 0_2 \rightarrow S\,i\,0_2\,(S)$ in oxygen

$S\,i\,(S) + H_2 0 \rightarrow S\,i\,0_2\,(S) + 2H_2$ in water rap our

High Preasure Oxidation

This process is applied to the oxide isolation of high speed bipolar LSI, with fully ion- implanted shallow junctions and multi-Level metallization

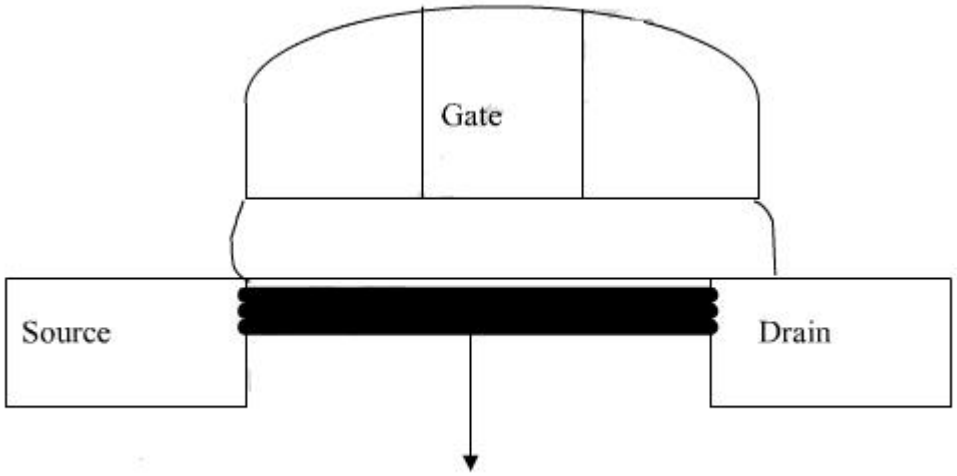
A shorter oxidation time for the thick field oxide brought about smaller redistribution of impurities of a buried collector, which resulted in almost 30% higher break down Voltage of devices.

Oxidation induced defects were greatly influenced with high pressure oxidation temperature.

Plasma Oxidation

The plasma oxidation involves the growth rather than deposition of high quality this Layers of silicon oxide at room temperature.

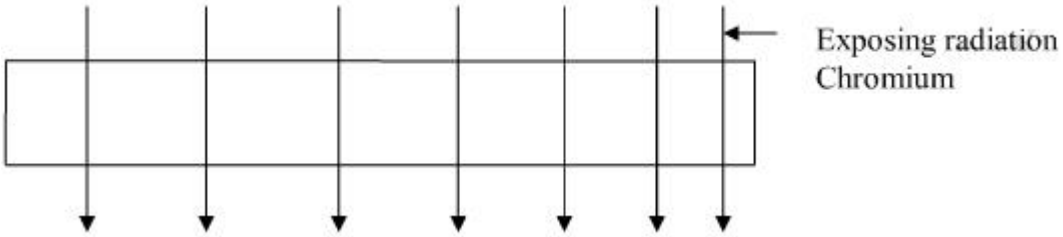
The technique employs the o produced in oxygen plasma.
and interfaces on SiGe alloys.

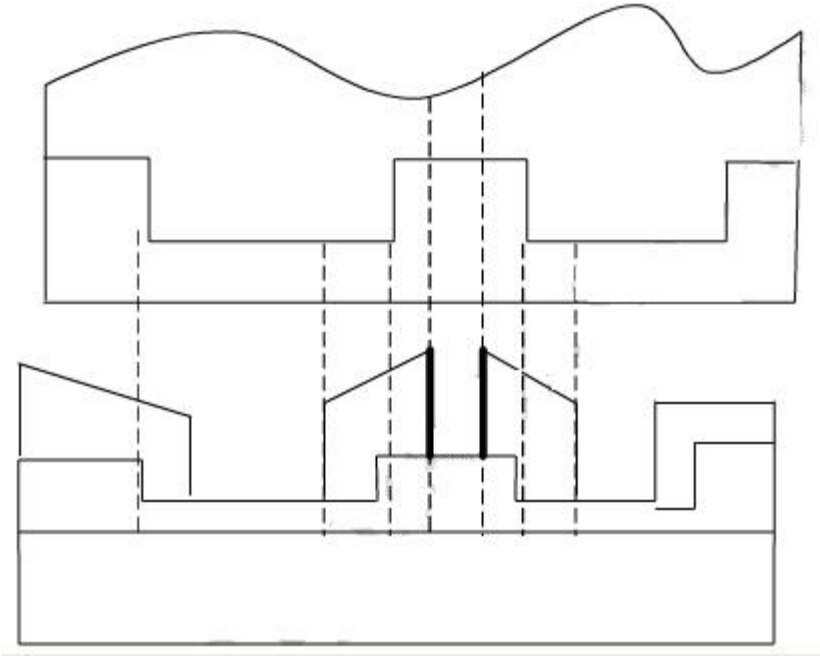


The gate oxide is grown by plasma oxidation. The SiGe channel cause enhancement of whole mobility.

LITHOGRAPHY

Lithography is one type of art made by impressing intern, several flat emborred Slabs each covered with greasy ink / Paint of definite colour onto a Paper. The figure below illustrates the Lithography process





In lithography for micromachining, the photosensitive material used is typically a photoresist (also called resist, other photosensitive polymers are also used). When resist is exposed to a radiation source of a specific a wavelength, the chemical resistance of the resist to developer solution changes. If the resist is placed in a developer solution after selective exposure to a light source, it will etch away one of the two regions (exposed or unexposed). If the exposed material is etched away by the developer and the unexposed region is resilient, the material is considered to be a positive resist (shown in figure 2a). If the exposed material is resilient to the developer and the unexposed region is etched away, it is considered to be a negative resist (shown in figure 2b).

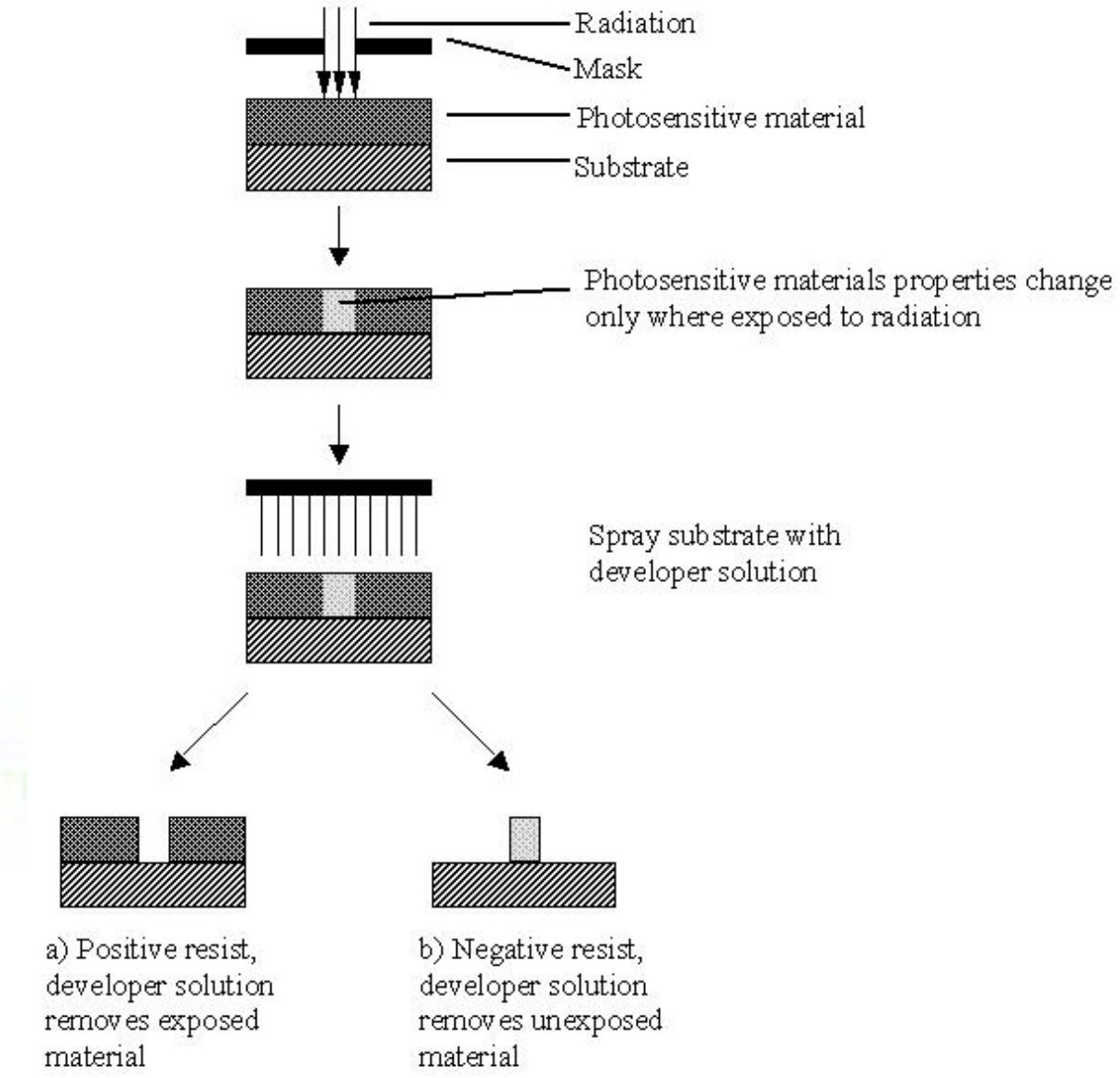


Figure 2: a) *Pattern definition in positive resist*, b) *Pattern definition in negative resist*

Diffusion

→ Diffusion is the process of introducing controlled amounts of do pants into semiconductors.

→ Using diffusion, conductivity of silicon is being altered by producing either n – type of p – type region.

→ Selectively by producing n – type and P – type regions required that diffusion to be carried out at an elevated temperature and by placing the do pant atoms on the surface of the do pant semiconductor.

→ So we have a high concentration of do pant at the surface and if gradually decreases as one move inside the semiconductor.

→ Diffusion is carried out in a furnace, Placing the wafers inside it and passing an inert I as that contains the desired do pant through it at an increased temperate in the range of 800 – 1200 ^{0}C

INTRODUCTION:

The basic characteristics of MOS transistor and the various possibilities of configuring inverter circuits are explained in this unit BiCMos transistors are also considered.

The expressions and discussion is done for nMos transistors and the PMOS expressions given polarities of nMos expressions. The exchange of μ_n for μ_p and electrons for holes will result in PMOS from η MOS expressions.

DRAIN TO SOURCE CURRENT I_{ds} VERSUS VOLTAGE V_{ds} RELATIONSHIPS:-

UNIT-2

Basic Electrical properties of MOS transistors

When a voltage is applied on the gate of a MOS transistor a charge is induced in the channel between source and drain. This charge moves from source to drain when a voltage V_{ds} is applied between drain and source. I_{ds} is dependent on V_{gs} and V_{ds}

$$I_{ds} = -I_{sd} = \frac{charginducedinchannel(QC)}{Electrontransittime(T)} \quad \text{(1)}$$

$$\text{Transit time } \tau_{sd} = \frac{Lengthofchannel(L)}{velocity(v)} \quad \text{(2)}$$

Where $v = \mu E_{ds}$

μ = Electron or hole mobility

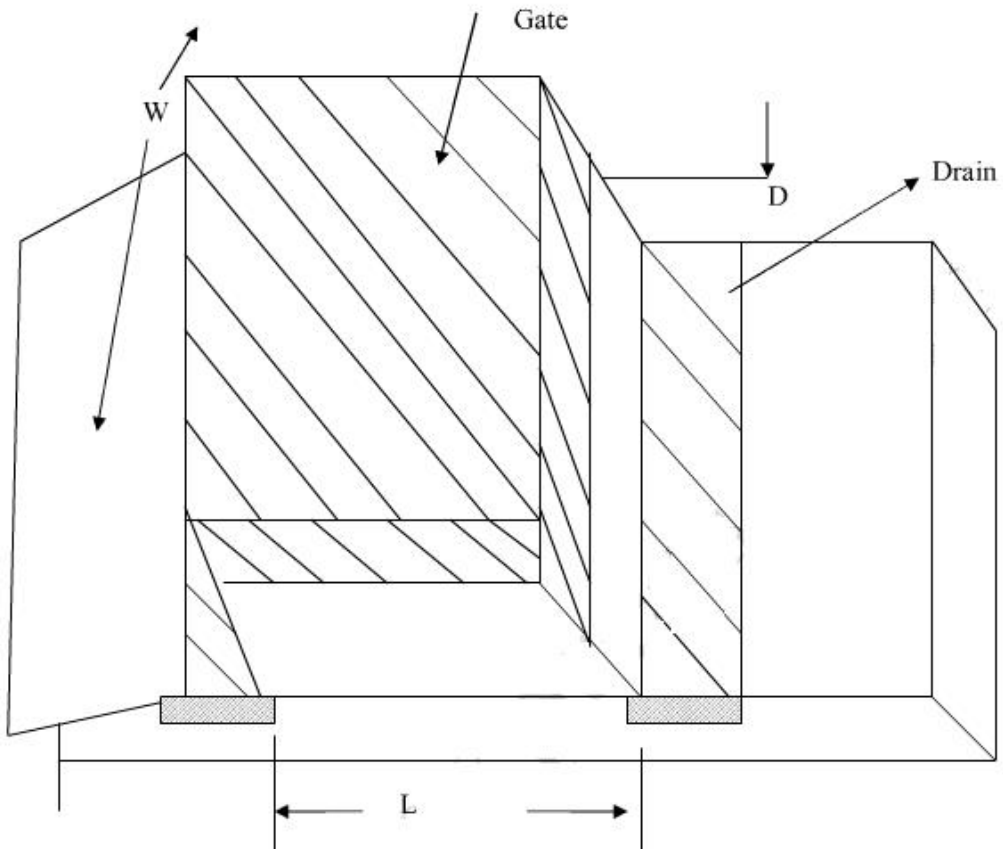
E_{ds} = electric field (drain to source)

We have $E_{ds} = \frac{V_{ds}}{L}$

So $v = \frac{\mu V_{ds}}{L}$

Substituting v in (2)

$$\tau_{sd} = \frac{L^2}{\mu V_{ds}}$$



Derivation for I_{ds}:-

1. Non-Saturated Region:-

As in non saturated region

$V_{ds} < V_{gs} - V_t$

As said in the previous section charge is induced in the channel and we have

Charge/unit area=Eg $\varepsilon ins\, \varepsilon_o$

$$Q_c = Eg\, \varepsilon ins\, \varepsilon_o . \frac{WL}{unitarea} \quad \text{_____(3)}$$

εins =relative permittivity of insulation between gate and channel

ε_o = permittivity of free space

$\varepsilon_o = 8.85 \times 10^{-14} Fcm^{-1}$

We have Eg = $\dfrac{\left[\left(V_{gs}-V_t\right)-\dfrac{V_{ds}}{2}\right]}{D}$

D = onide thickness

$\therefore$ Substituting Eg in (3) we get

$$Q_c = \frac{WL\varepsilon ins\varepsilon_o}{D}\left[\left(V_{gs}-V_t\right)-\frac{V_{ds}}{2}\right]$$

Substituting Q_c in equation (1)-$I_{ds} = \dfrac{Q_c}{\tau}$

We get

$$I_{ds} = \frac{\varepsilon ins\varepsilon_o\mu}{D}\frac{W}{L}\left[\left(V_{gs}-V_t\right)-\frac{V_{ds}}{2}\right]V_{ds}$$

$$= \mathbf{k}.\frac{W}{L}\left[\left(V_{gs}-V_t\right)V_{ds}-\frac{V_{ds}^{\,2}}{2}\right]$$

We take $\beta = K.\dfrac{W}{L}$

$$\therefore I_{ds} = \beta\left[\left(V_{gs}-V_t\right)V_{ds}-\frac{V_{ds}^{\,2}}{2}\right]$$

We also have gate channel capacitance

$$Cg = \frac{\varepsilon ins\varepsilon_o W.L}{D}$$

So $\quad K = \dfrac{Cg.\mu}{WL}$

$$\therefore I_{ds} = \frac{Cg\mu}{L^2}\left[\left(V_{gs}-V_t\right)V_{ds}-\frac{V_{ds}^{\,2}}{2}\right]$$

2. In saturated region we have

$$V_{ds} = V_{gs}\text{-}V$$

$$\therefore I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2$$

$$= \frac{Cg\mu}{2L^2}(V_{gs} - V_t)^2$$

MOS TRANSISTOR THRESHOLD VOLTAGE V_t:-

The charges stored in the dielectric layers and in the surface to surface interfaces ar neutralized by switching and enhancement mode transistor from off to on by applyi sufficient gate voltage

The threshold voltage V_t may be expressed as

$$V_t = \phi_{ms} \frac{Q_B - Q_{ss}}{C_o} + 2\phi_{fN}$$

Q_B = charge per unit area in the depletion layer beneath the oxide

Q_{ss} = charge density at $Si+SiO_2$ interface.

C_o = Capacitance per unit gate area

Q_{ms} = Work function difference gate and Si

Q_{fN} = Fermi level potential between inverted surface and bulk Si.

For PolySilicon gate and Silicon substrate the is determined as follows

$$Q_B = \sqrt{2\varepsilon_o \varepsilon_{si} qN(2\phi_{fN} + V_{SB})} coloumb/m^2$$

$$\phi_{fN} = \frac{KT}{q} \ln \frac{N}{ni} volts$$

$Q_{ss} = (1.5x10^8)x10^{-8}$colomb/$m^2$

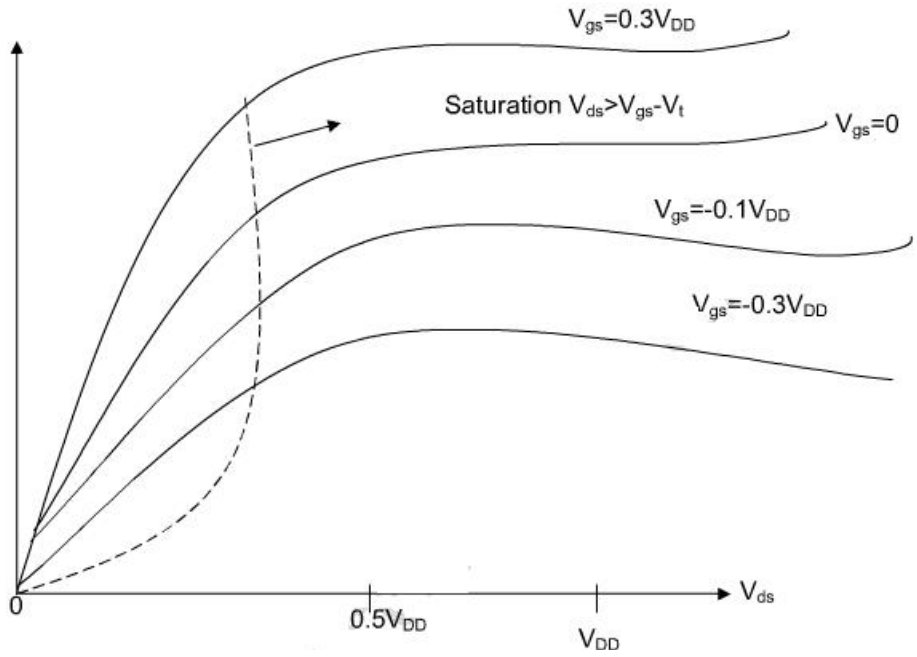
Where V_{SB} = Substrate bias voltage, $q=1.6x10^{-19}$coloumb,

N – impurity permittivity of silicon

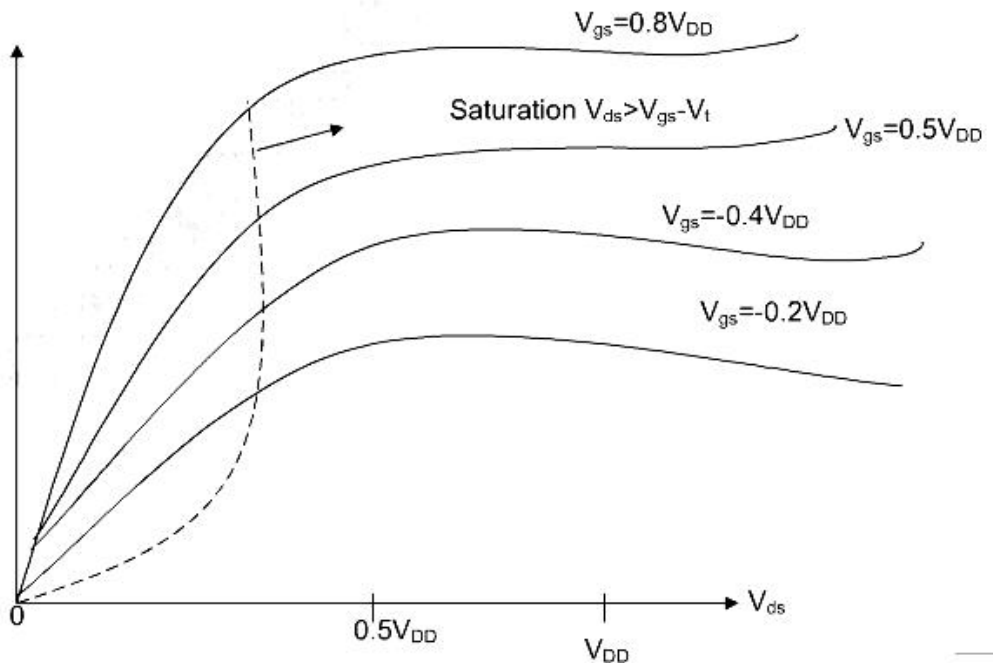
ε_{Si} – relative permittivity of Silicon

MOS transistor Characteristics

(a) Depletion mode device:-

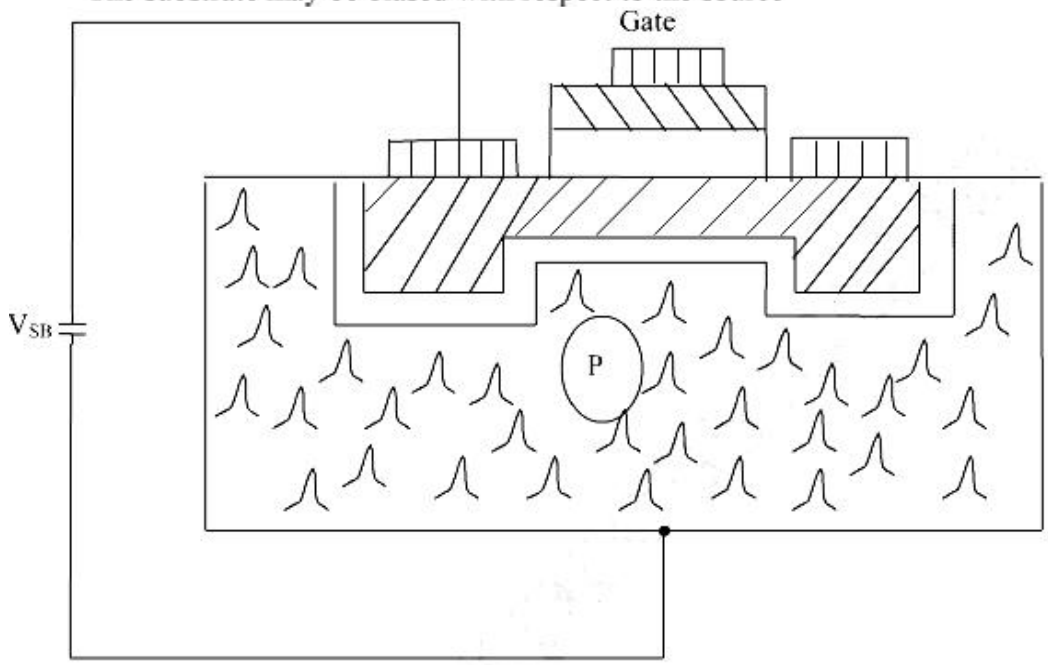


(b)Enhancement mode device:



BODY EFFECT

The substrate may be biased with respect to the source



Body effect (nMOS device shown)

When V_{SB} is increased, the channel is depleted of charge carriers and thus the threshold voltage is raised

Threshold is give by voltage

$V_t = \gamma(V_{SB})^{\frac{1}{2}}$ where γ is a constant which depends on substrate doping. The body effect will be smaller if the substrate is doped lightly

It also be written as

$$V_t = V_t(0) + \left[\frac{D}{\varepsilon ins\,\varepsilon_o}\right]\sqrt{2\varepsilon_o \varepsilon SiQN}\,(V_{SB})^{\frac{1}{2}}$$

Where $V_t(0)$ is the threshold voltage for $V_{SB}=0$

MOS TRANSISTOR TRANSCONDUCTANCE gm

Trans conductance expresses the relationship between output current I_{ds} and input voltage V_{gs} and is defined as

$$I_m = \frac{\delta I_{ds}}{\delta V_{gs}} \Big|_{V_{ds}=constant}$$

We have $\frac{Q_c}{I_{ds}} = \tau$

$$\therefore \delta I_{ds} = \frac{\delta Q_c}{\tau_{ds}}$$

Substituting $\tau_{ds} = \frac{L^2}{\mu V_{ds}}$ in above equation

$$\delta I_{ds} = \frac{\delta Q_c . \mu . V_{ds}}{L^2}$$

But $\delta Q_c = Cg . \delta V_{gs}$

So $\delta I_{ds} = \frac{C_g \delta V_{gs} . \mu . V_{ds}}{L^2}$

Now $g_m = \frac{\delta I_{ds}}{\delta V_{gs}} = \frac{Cg . \mu . V_{ds}}{L^2}$

In saturation $V_{ds} = V_{gs} - V_t$

$$g_m = \frac{C_g . \mu}{L^2}(V_{gs} - V_t)$$

Substituting $C_g = \frac{\varepsilon ins \varepsilon_o WL}{D}$

$$gm = \frac{\mu \varepsilon \sin \varepsilon_o}{D} . \frac{W}{L}(V_{gs} - V_t)$$

$$\Rightarrow gm = \beta(V_{gs} - V_t)$$

Output CONDUCTANCE g_{ds}

It can be expressed as

$$g_{ds} = \frac{\delta I_{ds}}{\delta V_{gs}} = \lambda . I_{ds} \propto \left(\frac{1}{L}\right)^{Z}$$

$$\lambda \propto \frac{1}{L} and I_{ds} \propto \frac{1}{L} for a \text{ MOS device.}$$

MOS TRANSISTOR FIGURE OF MERIT

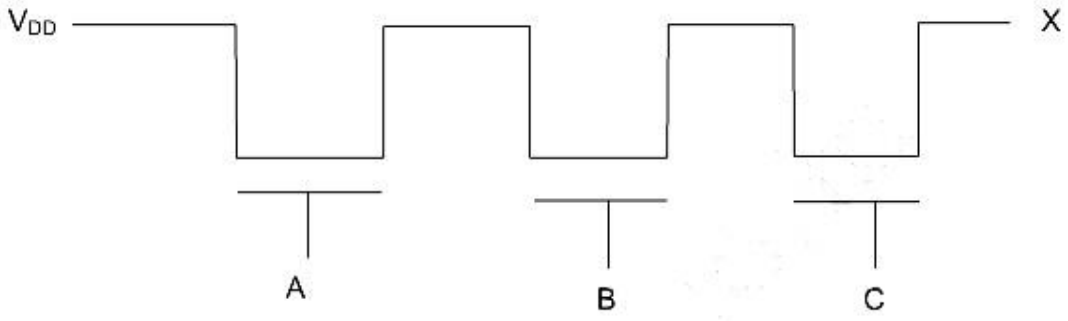
The parameter w_o is useful to find the frequency response.

$$w_o = \frac{g_m}{C_g} = \frac{\mu}{L^2}(V_{gs} - V_t)\left[= \frac{1}{\tau_{sd}} \right]$$

gm should be as high as possible for a fast circuit. Switching speed is determined by w_o

PASS TRANSISTOR

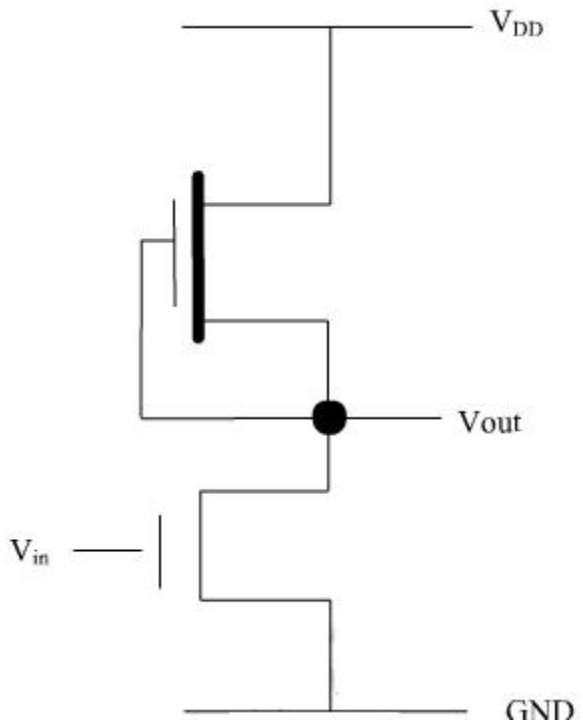
MOS transistors can be used as switches in series. This application is called as pass transistor. The and away is shown below



X = A.B.C (Logic 1= V_{DD}-V_t)

NMOS INVERTER

The inverter circuit consists of transistor with source connected to ground and a depletion mode transistor acting as a load resistor, connected between Drain and V_{DD}.



NMOS inverter

We have

The depletion mode transistor always on because gate is connected to source

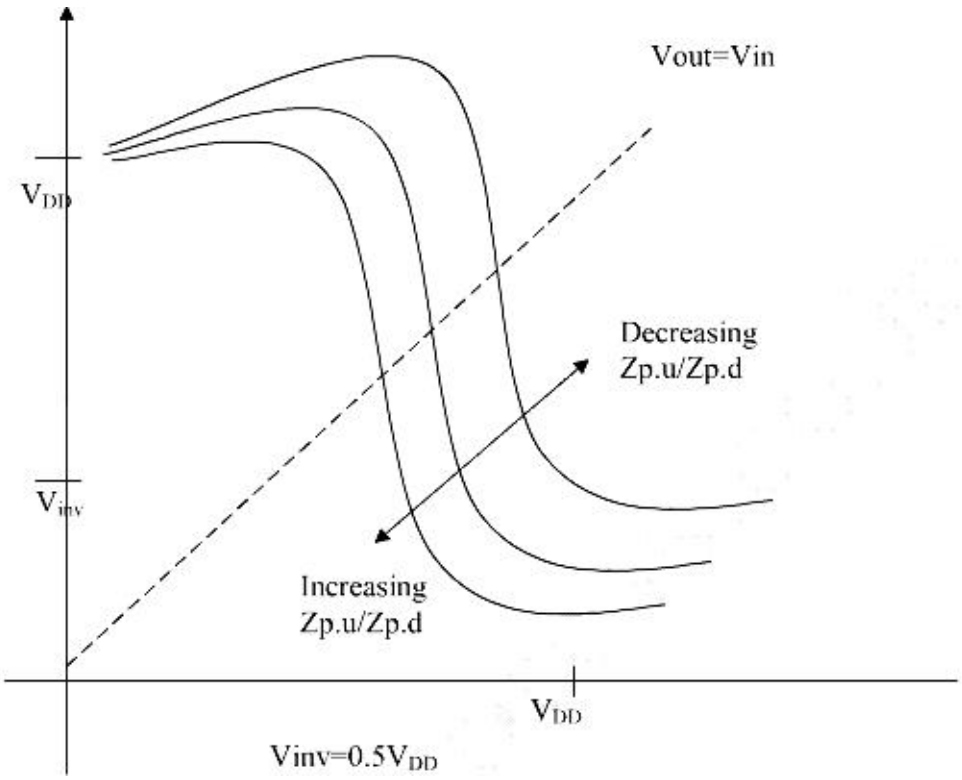
The depletion mode transistor is called pull up device and enhancement mode device is called pull down transistor

The inverter transfer characteristic is obtained by superimposing V_{gs}=0 depletion mode characteristic curve on family of waves for enhancement mode device

The points of intersection give the transfer characteristic

When V in exceeds the p.d threshold voltage current begin to flow

vout



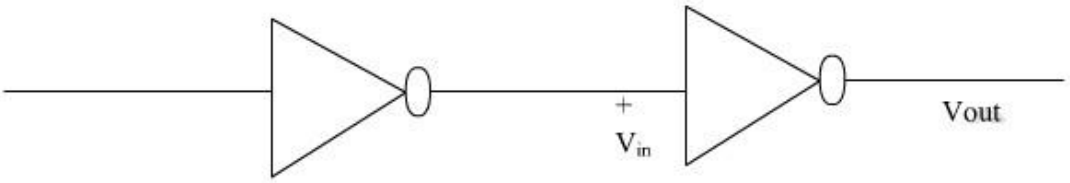
NMOS inverter transfer characterstic

Slope of the transfer characteristic determines the gain

$$\text{Gain} = \frac{\delta Vout}{\delta Vin}$$

PULL UP TO PULL DOWN RATIO (Zp.u/Zp.d) FOR nMOS INVERTER DRIVEN BY ANOTHER nMOS INVERTER

Consider the cascaded inverters in the figure below.



We assume $V_{in}=V_{out}=V_{inv}$

At a point $V_{inv}=0.5V_{DD}$ both the transistors are in saheration and

$$I_{ds} = K.\frac{W}{L}\frac{(V_{gs}-V_t)^2}{2}$$

In the depletion mode

$$I_{ds} = K.\frac{W_{p.u}}{L_{p.u}}\frac{(-V_{td})^2}{2}\sin ceV_{gs}=0$$

And in enhancement mode

$$I_{ds} = K.\frac{W_{p.d}}{L_{p.d}}\frac{(V_{inv}-V_t)^2}{2}\sin ceV_{gs}=V_{inv}$$

Equating (since currents are same) we have

$$\frac{W_{p.d}}{L_{p.d}}(V_{inv}-V_t)^2=\frac{W_{p.u}}{L_{p.u}}(-V_{td})^2$$

Where $W_{p.d}$, $L_{p.d}$, $W_{p.a}$ and $L_{p.u}$ are widths and lengths of pull down and pull up transistors respectively.

Now

$$Z_{p.d}=\frac{L_{p.d}}{W_{p.d}};Z_{p.u}=\frac{L_{p.u}}{W_{p.u}}$$

We have

$$\frac{1}{Z_{p.d}}(V_{inv}-V_t)^2=\frac{1}{Z_{p.u}}(-V_{td})^2$$

$$V_{inv} = V_t - \frac{V_{td}}{\sqrt{Z_{p.u}/Z_{p.d}}}$$

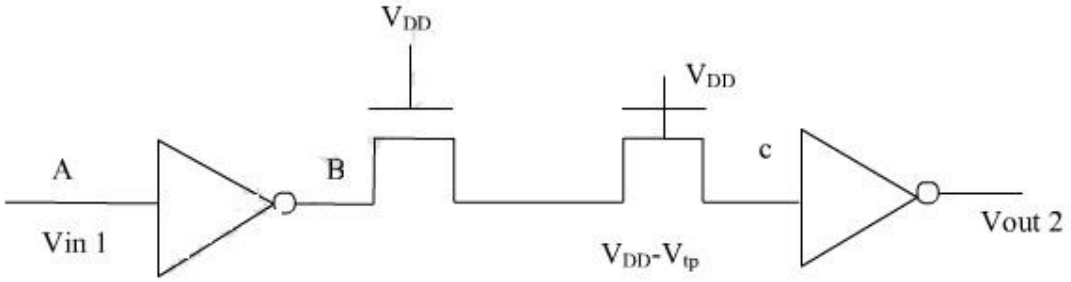
The typical values $V_t = 0.2V_{DD}$, $V_{td}=0.6V_{DD}$ and $V_{inv}=0.5V_{DD}$ are substituted in the above equation

$$\therefore 0.5 = 0.2 + \frac{0.6}{\sqrt{\frac{Z_{p.u}}{Z_{p.d}}}}$$

$$\sqrt{\frac{Z_{p.u}}{Z_{p.d}}} = 2$$

$$\frac{Z_{p.u}}{Z_{p.d}} = \frac{4}{1}$$

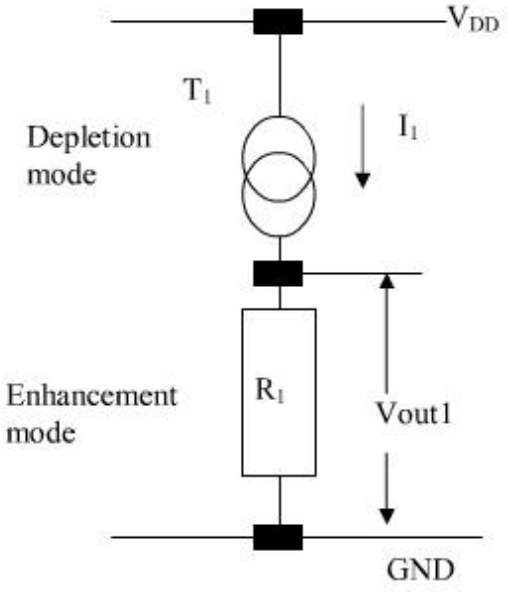
Pull up to Pull Down Ratio for an nMOS Inverter Driven Through One or More Pass Transistors:-



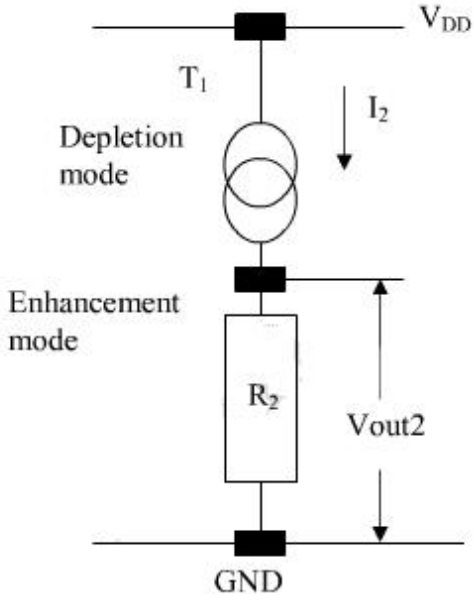
The connection of pass transistors will degrade the logic 1 level into inverter 2 so that the output 0 will not be a proper logic 0 level

When $V_{int}=0$ voltage at B = V_{DD}

And Input at C = $V_{in2} = V_{DD}-V_{tp}$
Where V_{tp} = threshold voltage for a pass transistor.



(a) Inverter 1 with input = V_{DD}



(b) Inverter 2 with Input = V_{DD}-V_{tp}

Equivalent Circuits of inverters 1 and 2

For the p.d transistor

$$I_{ds} = K.\frac{W_{p.d1}}{L_{p.d1}}\left[(V_{DD} - V_t)V_{ds1} - \frac{V^2_{ds1}}{2}\right]$$

Therefore

$$R_1 = \frac{V_{ds1}}{I_{ds}} = \frac{1}{K}.\frac{L_{p.d1}}{W_{p.d1}}\left[\frac{1}{V_{DD} - V_t - \frac{V_{ds1}}{2}}\right]$$

For depletion mode transistor in saturation with V_{gc} = (

$$I_1 = I_{ds} = K.\ \frac{W_{p.e1}}{L_{p.e1}}\frac{(-V_{td})^2}{2}$$

The product $I_1R_1 = V_{out}1$

$$\text{Vout1} = I_1 R_1 = \frac{Zp.d1}{Zp.u.1}\left[\frac{1}{V_{DD} - V_t}\right]\frac{(-V_{td})^2}{2}$$

When input = V_{DD}-V_{tp}

$$R_2 = \frac{1}{K}.Zp.dZ\frac{1}{(V_{DD} - V_{tp}) - V_t}$$

$$I_2 = K.\ \frac{1}{Zp.uZ}\frac{(-V_{td})^2}{2}$$

$$\text{Vout2} = I_2 R_2 = \frac{Zp.d2}{Zp.u2}\left[\frac{1}{V_{DD} - V_{tp} - V_t}\right]\frac{(-V_{td})^2}{2}$$

The necessary condition is

Vout1 = Vout2

There fore

$$\frac{Zp.u.2}{Zp.d.2} = \frac{Zp.u.1}{Zp.d.1}.\frac{(V_{DD} - V_t)}{(V_{DD} - V_{tp} - V_t)}$$

Taking typical values

$V_t = 0.2V_{DD}$

$V_{tp} = 0.3V_{DD}$

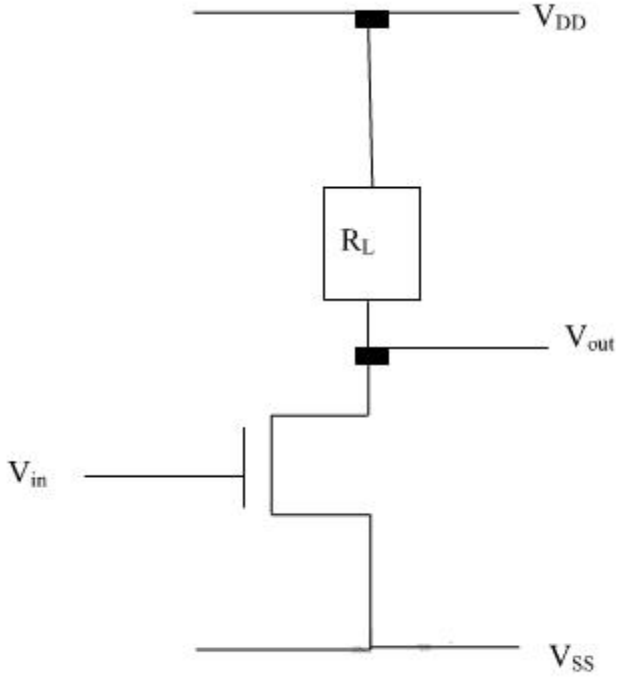
$$\frac{Zp.u.2}{Zp.d.2} = \frac{Zp.u.1}{Zp.d.1}.\frac{0.8}{0.5}$$

$$\frac{Zp.u.2}{Zp.d.2} \approx 2.\frac{Zp.u.1}{Zp.d.1} = 2\frac{4}{1} = \frac{8}{1}$$ (Approximately equal)

ALTERNATIVE FORMS OF PULL-UP

Load-Resistance RL

Resistors take large space. So they are not often used.



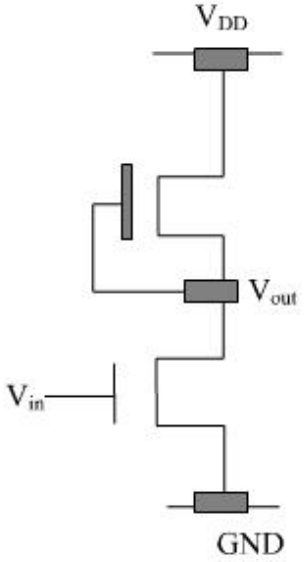
(GND

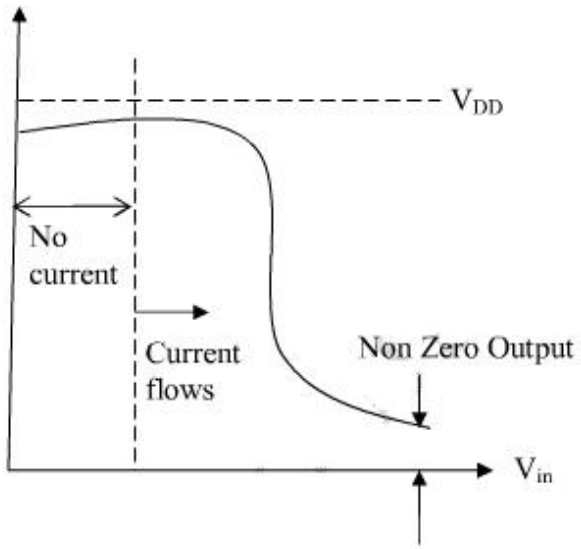
Resistor Pull-up

nMOS Deletion Mode Transistor Pull-Up

(a) Dissination is high when V_{in} = logical,

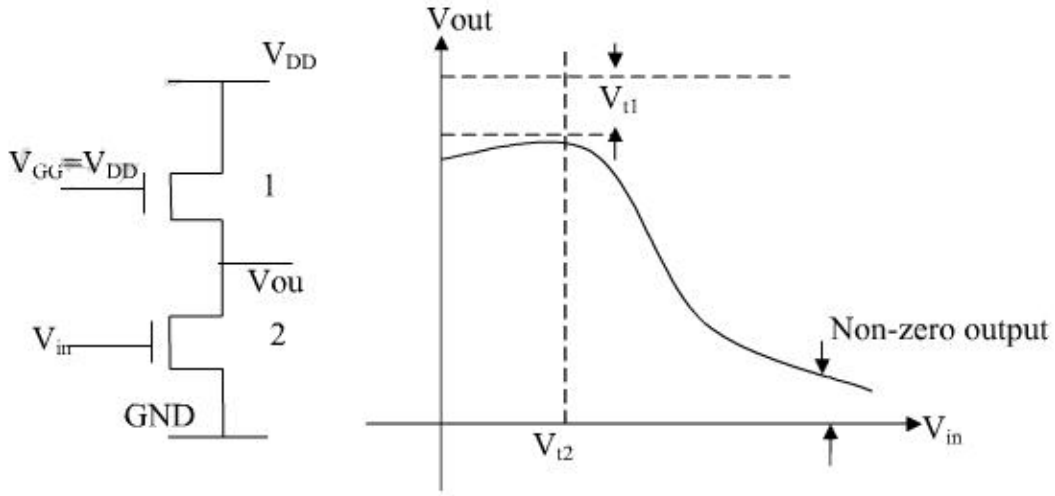
(b) Switch of output from 1 to 0 begins when V_{in} exceeds V_t of p.d device





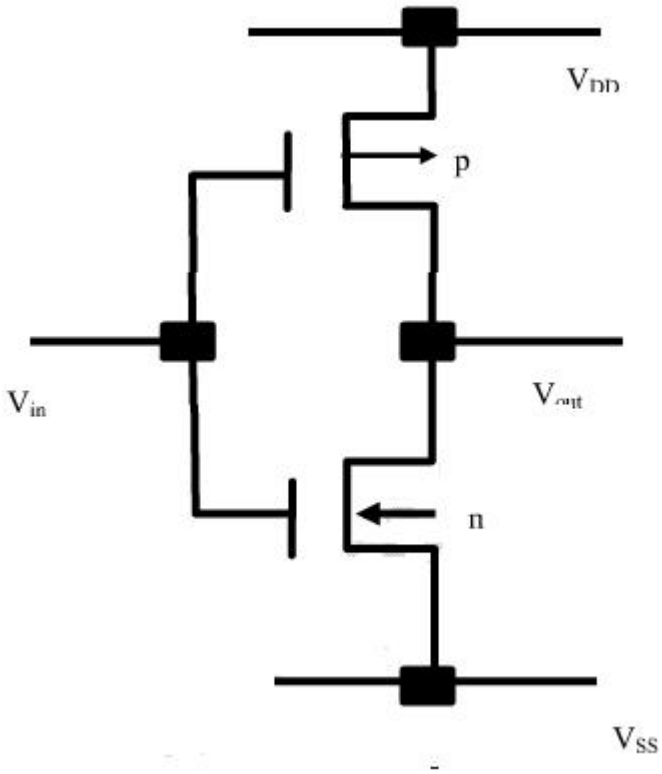
nMOS Enhancement Mode Pull-Up

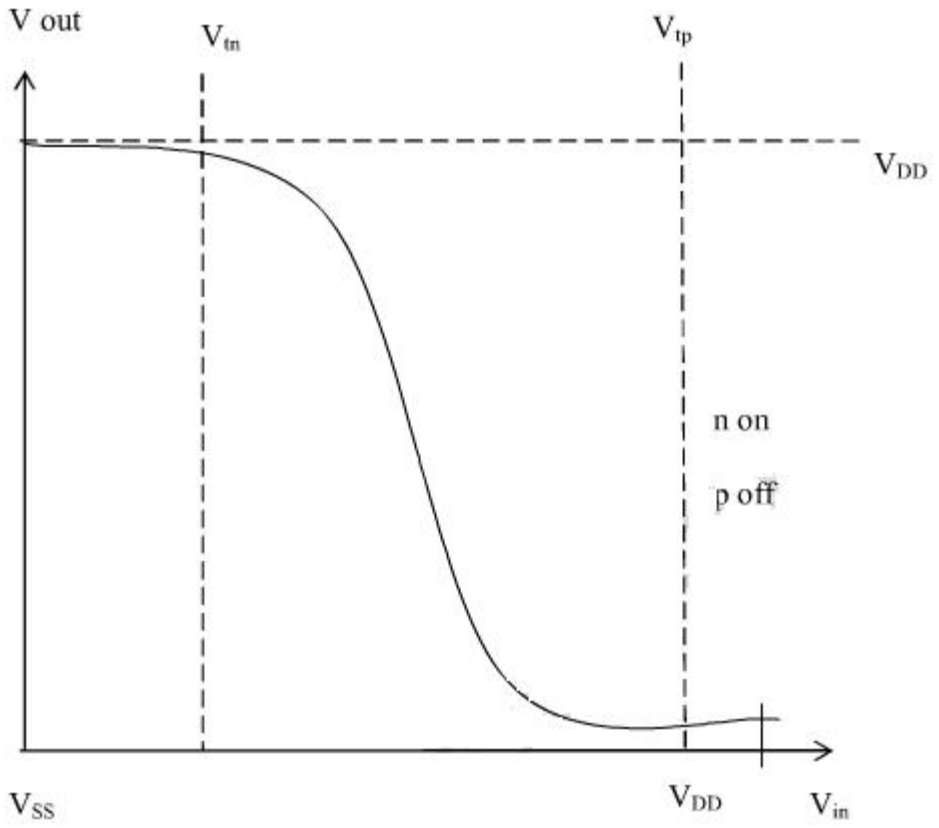
(a) Dissipation is high since current flows when V_{in} = logical 1 (V_{GG} is returned to V_{DD}).
(b) V_{out} can never reach V_{DD}.



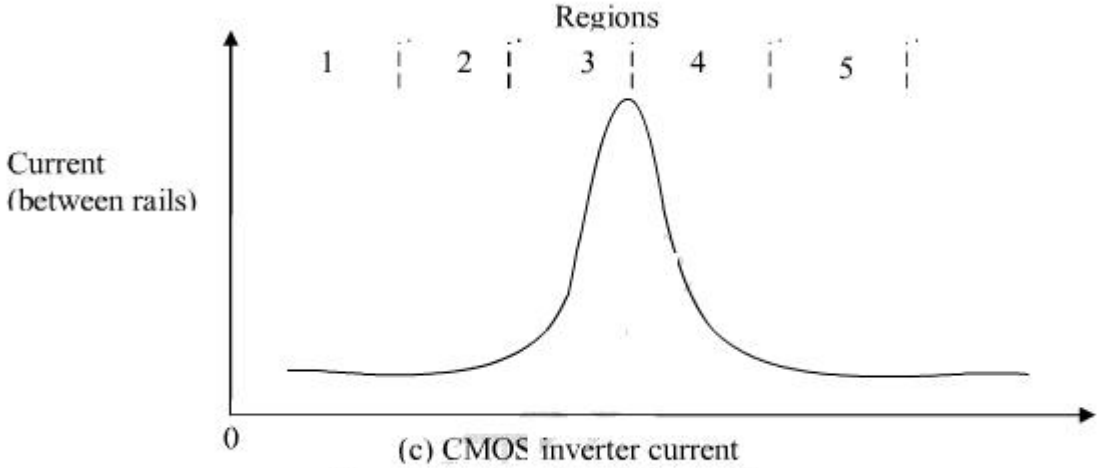
Complementary Transistor Pull-up (CMOS)

(a) No current flow for both logical 0 and 1 inputs.
(b) Iull logical 1 and 0 levels are presented at output.





(b) Transfer Characteristic



(c) CMOS inverter current

Complementary transistor pull-up

CMOS INVERTER ANALYSIS AND DESIGN

The connection and characteristics are shown in above diagram. In the resistive region

$$I_{ds} = K.\frac{W}{L}(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^{\ 2}}{2}$$

In the saturation region

$$I_{ds} = K.\frac{W}{L}\frac{(V_{gs} - V_t)^2}{2}$$

$$B = K\frac{W}{L}$$

β may be applied to both nMOS and p-MOS transistors

$$\beta_n = \frac{\varepsilon ins\varepsilon_o\mu_n}{D}.\frac{W_n}{L_n}$$

$$\beta_p = \frac{\varepsilon ins\varepsilon_o\mu_p}{D}.\frac{W_p}{L_p}$$

In region 5, V_{in} = 1 and Vout = 0. In region 1 V_{in}=logic 0 and V_{out}=1.

Here p-transistor is fully turned ON and n-transistor is fully turned off.

In region 2, the analysis is done by equating p-device resistive region current with n-device saturation current. Region 4 is similar to region 2 with the functions of p and n transistors reversed.

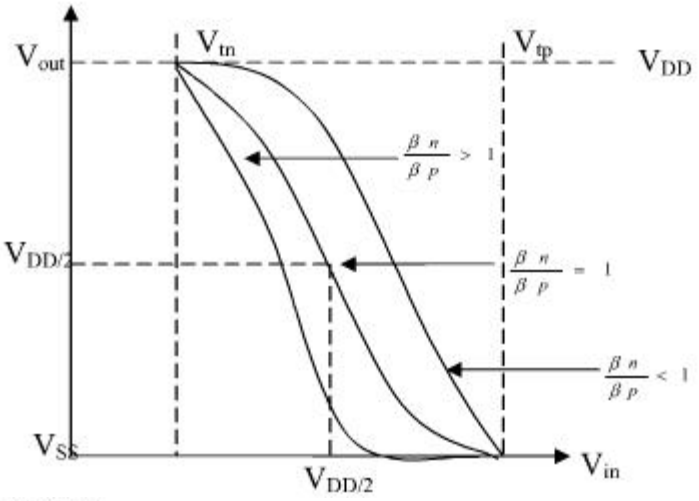
The currents must be the same in each device, so

$$I_{dsp} = -I_{dsn}$$

$$\frac{B_p}{Z}(V_{in} - V_{DD} - V_{tp})^2 = \frac{\beta_n}{2}(V_{in} - V_{tn})^2$$

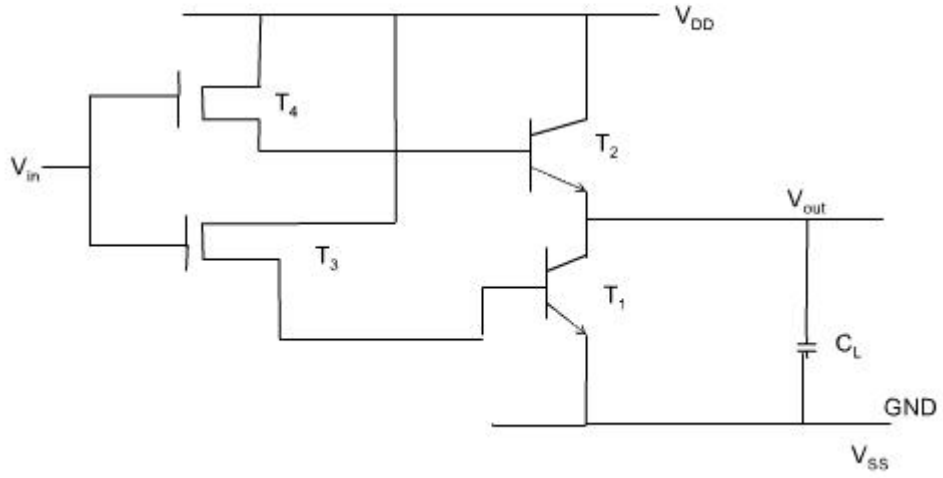
$$\therefore V_{in} = \frac{V_{DD} + V_{tp} + V_{tn}(\beta_n/\beta_p)^{\frac{1}{2}}}{1 + (\beta_n/\beta_p)^{1/2}}$$

The transfer characteristic with β ratio is shown in the figure below.



BI-CMOS INVERTERS

A simple BiCMOS inverters circuit is shown in the following figure



Bipolar transistors are used to drive the output loads

When $V_{in} = 0$, T_3 and T_1 all off, T_4 and T_2 are on and $V_{out} = +5V$

When $V_{in} = +5V$, T_4 and T_2 are off and T_3 and T_1 are on so the capacitor C_L is discharged to o volts

Characteristics

The inverter has high input impedance
The inverter has low output impedance
It has high noise margins
It occupies relatively small area.