Code: 15A04604 **R15**

B.Tech III Year II Semester (R15) Supplementary Examinations December/January 2018/19

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Differentiate between PMOS and NMOS transistors.

(b) Write the basic DC equations of a MOS transistor design in cutoff, saturation and linear region.

(c) Find the sheet resistance of a material, given the resistivity $\rho = 21\Omega m$ and the thickness is 3m.

(d) Give some limitations of scaling.

(e) Define the terms placement of scaling.

(f) Give comparison of clock routing and power routing.

(g) What is the use of a comparator? Draw the simple comparator circuit?

(h) Differentiate between standard cells and gate arrays.

(i) Define the terms synthesis and simulation.

(j) Why do we need "Design for testability" in a VLSI design?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain in detail about the steps involved in SOI technology fabrication process with essential diagrams.

OR

3 Design a CMOS inverter circuit and explain about its various regions of operation in detail with the necessary diagrams.

UNIT – II

4 With necessary equations, explain in detail about simple capacitive model and flat band capacitance model.

OR

5 (a) Discuss about VLSI design flow.

(b) Write short notes on stick diagram and layout diagram.

UNIT – III

6 With a detailed step by step process, design and draw the OR-AND-INVERT form complex gates in CMOS logic for the output expression Y = $\overline{\left((A+B).(C+D)\right)}$.

OR

7 List out the types of routing in a CMOS physical design. And give a detailed note on each one of them.

UNIT – IV

8 Draw the truth table for a carry look ahead adder. With the help of K-map reduce the equation and draw the logical circuit diagram for the obtained equation.

OR

9 Discuss about design approach of Full custom and Semi-custom devices.

UNIT – V

10 Write a short note on the following tools:

(a) Design capture tools.

(b) Design verification tools.

OR

11 Explain in detail about Fault modeling and simulation with the necessary example circuits.

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Code: 15A04604

SS

B.Tech IV Year I Semester (R15) Regular Examinations November/December 2018

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Mention different MOS layers.
(b) Give the basic process for IC fabrication.
(c) When the channel is said to be pinched-off?
(d) Give the various color codings used in stick diagram.
(e) Define threshold voltage in CMOS.
(f) List the two components of power dissipation.
(g) Define the structural gate-level modeling.
(h) Mentions different methods of programming of PALs.
(i) What is the standard cell-based ASIC design?
(j) What are the different levels of design abstraction at physical design?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Explain the CMOS n-well fabrication process indicating the masks used.
(b) Mention the significance of threshold voltage of a MOS device.

OR

3 (a) Compare CMOS and Bipolar technologies.
(b) Explain the NMOS fabrication procedure.

UNIT – II

4 (a) Discuss and compare the CMOS design style and nMOS design style.
(b) Design stick diagram for nMOS two input NAND and NOR gates.

OR

5 (a) Illustrate the lambda-based design rules with neat sketches.
(b) Design a layout diagram for the CMOS logic function: $Y = \overline{A + B + C}$.

UNIT – III

6 Describe the power delay estimation in the view of physical design.

OR

7 Draw the complete layout diagram of NAND gate and give the procedural steps for drawing the same.

UNIT – IV

8 Explain the design of a 4-bit shifter in detail.

OR

9 (a) Discuss the general arrangement of a 4-bit arithmetic process.
(b) Write about FPGA programming technologies in detail.

UNIT – V

10 (a) Design a queue and write the dataflow style VHDL program for the same.
(b) Describe VHDL synthesis approach with an example.

OR

11 (a) List various VHDL verification tools and explain any one of them.
(b) Compare different design verification tools.

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