G. Pullaiah College of Engineering and Technology

(Autonomous)

(Approved by AICTE | NAAC Accreditation with 'A' Grade | Accredited by NBA (ECE & EEE) | Affiliated to JNTUA)

Nandikotkur Road, Venkayapalli (V), Kurnool – 518452, Andhra Pradesh

MASTER OF TECHNOLOGY
Digital Electronics & Communication Systems

ACADEMIC REGULATIONS GPCET – R25

M.Tech Regular Two Year Degree Programme

(for the batches admitted from the academic year 2025-26)

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Academic Regulations of M.Tech. (Full Time/Regular) Programme

(Effective for the students admitted into I year from the Academic Year 2024-25 and onwards)

G.Pullaiah College of Engineering and Technology, Kurnool offers **Two** Years (**Four** Semesters) full-time Master of Technology (M.Tech.) Degree programme, under Choice Based Credit System (CBCS) in different branches of Engineering and Technology with different specializations.

The G.Pullaiah College of Engineering and Technology, Kurnool shall confer M. Tech. degree on candidates who are admitted to the programme and fulfill all the requirements for the award of the degree.

1. **Award of the M.Tech. Degree**

   A student will be declared eligible for the award of the M.Tech. degree if he/she fulfills the following:

   1.1 Pursues a course of study for not less than two academic years and not more than four academic years.

   1.2 Registers for 75 credits and secures all 75 credits.

2. Students, who fail to fulfill all the academic requirements for the award of the degree within four academic years from the year of their admission, shall forfeit their seat in M.Tech. course and their admission stands cancelled.

3. **Programme of Study:**

   The following M.Tech. Specializations are offered at present in different branches of Engineering and Technology.

S.No.	Discipline	Name of the Specialization	Code
01	Electrical and Electronics Engineering	Electrical Power Systems	07
02	Electronics and Communication Engineering	Digital Electronics & Communication Systems	38
03	Computer Science and Engineering	Computer Science & Engineering	58

4. **Eligibility for Admissions**:

   4.1 Admission to the M. Tech Program shall be made subject to the eligibility, qualification and specialization prescribed by the A.P. State Government/University from time to time.

   4.2 Admissions shall be made either on the basis of the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by A.P. State Government (APPGECET) for M.Tech. programmes an entrance test conducted by University/on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.

5. Programme related terms:

5.1 ***Credit:*** A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (Lecture/Tutorial) or two hours of practical work/field work per week.

Credit definition:

1 Hr. Lecture (L) per week	1 credit
1 Hr. Tutorial (T) per week	1 credit
1 Hr. Practical (P) per week	0.5 credit

5.2 ***Academic Year:*** Two consecutive (one odd + one even) semesters constitute one academic year.

5.3 ***Choice Based Credit System (CBCS):*** The CBCS provides choice for students to select from the prescribed courses.

6. Programme Pattern:

6.1 Total duration of the M.Tech. programme is two academic years

6.2 Each academic year of study is divided into two semesters.

6.3 Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per semester.

6.4 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M.Tech. degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M.Tech. programme.

6.5 The medium of instruction of the programme (including examinations and project reports) will be in English only.

6.6 All subjects/courses offered for the M.Tech. degree programme are broadly classified as follows:

S.No.	Broad Course Classification	Course Category	Description
1.	Core Courses	Foundational & Professional Core Courses (PC)	Includes subjects related to the parent discipline/department/branch of Engineering
2.	Elective Courses	Professional Elective Courses (PE)	Includes elective subjects related to the parent discipline/department/ branch of Engineering
		Open Elective Courses (OE)	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline which are of importance in the context of special skill development
3.	Mandatory Course	Quantum Technology and Application	To understand importance of latest technologies, research and process of creation of patents through research
		Research methodology & IPR	
4.	Research	Skill Enhancement courses (SE)	Interdisciplinary/job-oriented/domain courses which are relevant to the industry
		Comprehensive Viva	To test the overall domain knowledge
		Short Term Industry Internship	To provide real time exposure

		Dissertation	To provide application of domain knowledge to solve real problems
5.	Audit Courses	Mandatory noncredit courses	Covering subjects of developing desired attitude among the learners.

6.7 The college shall take measures to implement Virtual Labs (https://www.vlab.co.in) which provide remote access to labs in various disciplines of Engineering and will help student in learning basic and advanced concept through remote experimentation. Student shall be made to work on virtual lab experiments during the regular labs.

6.8 A faculty advisor/mentor shall be assigned to each specialization to advise students on the programme, its Course Structure and Curriculum, Choice of Courses, based on his competence, progress, pre-requisites and interest.

6.9 Preferably 25% course work for the theory courses in every semester shall be conducted in the blended mode of learning.

7. Attendance Requirements:

7.1 A student shall be eligible to appear for the University external examinations if he/she acquires i) a minimum of 50% attendance in each course and ii) 75% of attendance in aggregate of all the courses.

7.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee.

7.3 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence

7.4 Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that class.

7.5 A stipulated fee shall be payable towards condonation of shortage of attendance.

7.6 A student will not be promoted to the next semester unless he satisfies the attendance requirements of the present semester. They may seek re-admission into that semester when offered next.

7.7 If any candidate fulfils the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

7.8 If the learning is carried out in blended mode (both offline & online), then the total attendance of the student shall be calculated considering the offline and online attendance of the student.

8. Evaluation – Distribution and Weightage of Marks:

The performance of a student in each semester shall be evaluated subject - wise (irrespective of credits assigned), for a maximum of 100 marks for theory and 100 marks for practical, based on Internal Evaluation and End Semester Examination.

8.1 There shall be five units in each of the theory subjects. For the theory subjects 60 marks will be for the End Examination and 40 marks will be for Internal Evaluation.

8.2 Two Internal Examinations shall be conducted for 30 marks each, one in the middle of the Semester and the other immediately after the completion of instruction period. The other 10 marks is awarded for continuous assessment in the form of

assignments, quizzes, open book examination, presentation, etc. First mid examination shall be conducted for I & II units of the syllabus and second mid examination for III, IV & V units. Each mid exam shall be conducted for a total duration of 120 minutes with 3 questions (without choice) and each question carries 10 marks. Final Internal marks for a total of 40 marks shall be arrived at by considering the marks secured by the student in both the internal examinations with 80% weightage to the better internal exam and 20% to the other.

8.3 The following pattern shall be followed in the End Examination:

i. Five questions shall be set from each of the five units with either/or type for 12 marks each.
ii. All the questions have to be answered compulsorily.
iii. Each question may consist of one, two or more bits.

8.4 For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day-to-day performance.
The internal evaluation based on the day-to-day work-10 marks, record- 10 marks and the remaining 20 marks to be awarded by conducting an internal laboratory test.
The end examination shall be conducted by the examiners, with a breakup mark of Procedure-10, Experimentation-25, Results-10, Viva- voce-15.

8.5 There shall be Mandatory **Audit courses** in I & II semesters for zero credits. There is no external examination for audit courses. However, attendance shall be considered while calculating aggregate attendance and student shall be declared to have passed the mandatory course only when he/she secures 50% or more in the internal examinations. In case, the student fails, a re- examination shall be conducted for failed candidates for 40 marks for every six months/semester satisfying the conditions mentioned in item 1 & 2 of the regulations.

8.6 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

8.7 In case the candidate does not secure the minimum academic requirement in any of the subjects he/she has to reappear for the Semester Examination either supplementary or regular in that subject or repeat the course when next offered or do any other specified subject as may be required.

8.8 The laboratory records and mid semester test papers shall be preserved for a minimum of 3 years in the respective institutions as per the University norms and shall be produced to the Committees of the University as and when the same are asked for.

9. Credit Transfer Policy

As per University Grants Commission (Credit Framework for Online Learning Courses through SWAYAM) Regulation, 2016, the University shall allow up to a maximum of 40% of the Professional and Open Electives in a semester through SWAYAM/SWAYAM Plus.

9.1 The University shall offer credit mobility for MOOCs and give the equivalent credit weightage to the students for the credits earned through online learning courses through SWAYAM platform.

9.2 The online learning courses available on the SWAYAM platform will be considered for credit transfer. SWAYAM course credits are as specified in the platform

9.3 Student registration for the MOOCs shall be only through the institution, it is mandatory for the student to share necessary information with the institution

9.4 The institution shall select the courses to be permitted for credit transfer through SWAYAM. However, while selecting courses in the online platform institution would essentially avoid the courses offered through the curriculum in the offline mode.

9.5 The institution shall notify at the beginning of semester the list of the online learning courses eligible for credit transfer in the forthcoming Semester.

9.6 Students may register for an 8-week (2 credits) or 12-week (3 credits) SWAYAM / SWAYAM plus course with the approval of the Head of the Department (HoD).

9.7 Examination fees, if applicable, shall be borne by the student. Pass marks and grading will be as per the GPCET academic regulations.

9.8 A student must get minimum 40% marks for assignments and quizzes on the SWAYAM/ SWAYAM plus platform to be eligible for the end-semester examination. The students who are unable to get minimum internal marks in SWAYAM/ SWAYAM plus platform, they have to re-register for the course in subsequent semester through SWAYAM/ SWAYAM plus platform.

9.9 The end-semester exam may be conducted by the National Testing Agency (NTA), the National Programme on Technology Enhanced Learning (NPTEL) or the University during the regular end-term exams. Evaluation shall comprise 60% weightage for the end-semester examination and 40% for assignments and quizzes conducted by the SWAYAM/ SWAYAM plus course coordinator. The student has to get 50% marks for internal and external with minimum of 40% marks in the external examination to declare them as pass.

9.10 The institution shall also ensure that the student has to complete the course and produce the course completion certificate as per the academic schedule given for the regular courses in that semester. However, the credits will be transferred to the students who got minimum 50% marks with 40% marks in the external examination

9.11 The institution shall designate a faculty member as a Mentor for each course to guide the students from registration till completion of the credit course.

9.12 The university shall ensure no overlap of SWAYAM MOOC exams with that of the university examination schedule. In case of delay in SWAYAM results, the university will re-issue the marks sheet for such students.

9.13 Student pursuing courses under MOOCs shall acquire the required credits only after successful completion of the course and submitting a certificate issued by the competent authority along with the minimum 50% of marks and grades.

9.14 The institution shall submit the following to the examination section of the university:

a) List of students who have passed MOOC courses in the current semester along with the certificates of completion.

b) Undertaking form filled by the students for credit transfer.

9.15 The university shall resolve any issues that may arise in the implementation of this policy from time to time and shall review its credit transfer policy in the light of periodic changes brought by UGC, SWAYAM, NPTEL and state government.

Note: Students shall also be permitted to register for MOOCs offered through online platforms other than SWAYAM NPTEL. In such cases, credit transfer shall be permitted only after seeking approval of the University at least three months prior to the commencement of the semester.

10. Re-registration for Improvement of Internal Evaluation Marks:

A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and has failed in the end examination

10.1 The candidate should have completed the course work and obtained examinations results for **I, II and III** semesters.

10.2 The candidate should have passed all the subjects for which the Internal Evaluation marks secured are more than 50%.

10.3 Out of the subjects the candidate has failed in the examination due to Internal Evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.

10.4 The candidate has to re-register for the chosen subjects and fulfill the academic requirements.

10.5 For reregistration the candidates have to apply to the University through the college by paying the requisite fees and get approval from the University before the start of the semester in which re-registration is required

10.6 In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

11. Evaluation of Project/Dissertation Work:

The Project work shall be initiated at the beginning of the III Semester and the duration of the Project is of two semesters. Evaluation of Project work is for 300 marks with 200 marks for internal evaluation and 100 marks for external evaluation. Progress of the project work is monitored through three reviews:

- Project review – I at the beginning of the III semester for zero marks
- Project review – II at the end of the third semester for 100 marks
- Project review – III before submission of the thesis i.e., end of the IV semesters for 100 marks

External evaluation of final Project work viva voce in IV semester shall be for 100 marks.

A Project Review Committee (PRC) shall be constituted with the Head of the Department as Chairperson, Project Supervisor and one faculty member of the department offering the M.Tech. programme.

11.1 A candidate is permitted to register for the Project Work in III Semester after satisfying the attendance requirement in all the subjects, both theory and laboratory (in I & II semesters).

11.2 A candidate is permitted to submit Project dissertation with the approval of PRC. The candidate has to pass all the theory, practical and other courses before submission of the Thesis.

11.3 Project work shall be carried out under the supervision of teacher in the parent department concerned.

11.4 A candidate shall be permitted to work on the project in an industry/research organization on the recommendation of the Head of the Department. In such cases, one of the teachers from the department concerned would be the internal guide and an expert from the industry/ research organization concerned shall act as co-

supervisor/ external guide. It is mandatory for the candidate to make full disclosure of all data/results on which they wish to base their dissertation. They cannot claim confidentiality simply because it would come into conflict with the Industry's or R&D laboratory's own interests. A certificate from the external supervisor is to be included in the dissertation.

11.5 Continuous assessment of Project Work - I and Project Work – II in III & IV semesters respectively will be monitored by the PRC.

11.6 The candidate shall submit status report by giving seminars in three different phases (two in III semester and one in IV semester) during the project work period. These seminar reports must be approved by the PRC before submission of the Project Thesis.

11.7 After registration, a candidate must present in Project Review - I, in consultation with his Project Supervisor, the title, objective and plan of action of his Project work to the PRC for approval within four weeks from the commencement of III Semester. Only after obtaining the approval of the PRC can the student initiate the project work.

11.8 The Project Review - II in III semester carries internal marks of 100. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Project Work.

11.9 A candidate has to secure a minimum of 50% of marks to be declared successful in Project Review - II. Only after successful completion of Project Review – II, candidate shall be permitted for Project Work Review – III in IV Semester. The unsuccessful students in Project Review - II shall reappear after three months.

11.10 The Project Review - III in IV semester carries 100 internal marks. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The PRC will examine the overall progress of the Project Work and decide whether or not eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Review - III. If student fails to obtain the required minimum marks, he/she has to reappear for Project Review - III after a month.

11.11 For the approval of PRC the candidate shall submit the draft copy of dissertation to the Head of the Department and make an oral presentation before the PRC.

11.12 After approval from the PRC, the student is permitted to submit a report. The dissertation report will be accepted only when the plagiarism is within 30% checked through Turnitin software (repository mode). The plagiarism report shall be submitted along with the dissertation report.

11.13 Research paper related to the Project Work shall be published in an SCI/ESCI/Scopus/UGC Care listed journal, or in conference proceedings with ISBN number organized by professional societies such as IEEE, IEI, etc.

11.14 After successful plagiarism check and publication of research paper, three copies of the dissertation certified by the supervisor and HOD shall be submitted to the College.

11.15 The dissertation shall be adjudicated by an external examiner selected by the University. For this, the Principal of the College shall submit a panel of three examiners as submitted by the supervisor concerned and department head for each

student. However, the dissertation will be adjudicated by one examiner nominated by the University.

11.16 If the report of the examiner is not satisfactory, the candidate shall revise and resubmit the dissertation, in the time frame as decided by the PRC. If report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate has to reregister for the project and complete the project within the stipulated time after taking the approval from the University

11.17 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and make arrangements for the conduct of Project Viva voce exam.

11.18 The Project Viva voce examinations shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who has adjudicated the dissertation. For Dissertation Evaluation (Viva voce) in IV Sem. there are external marks of 100 and it is evaluated by external examiner. The candidate has to secure a minimum of 50% marks in Viva voce exam.

11.19 If he fails to fulfill the requirements as specified, he will reappear for the Project Viva voce examination only after three months. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree.

12 Industry Internships:

Industry internship either onsite or virtual with a minimum of 06-08 weeks" duration, done at the end of Ist year second semester. It shall be completed in collaboration with local industries, Govt. Organizations, construction agencies, Power projects, software MNCs or any industries in the areas of concerned specialization of the PG program. The student shall register for the internship as per course structure after commencement of academic year.

Evaluation of the summer internships shall be through the departmental committee. A student will be required to submit a summer internship report to the concerned department and appear for an oral presentation before the departmental committee comprising of Head of the Department, Mentor/Supervisor of the internship and a senior faculty member of the department. A certificate of successful completion from industry shall be included in the report. Internship will be evaluated for 100 marks with 50 marks for the report evaluated by the mentor and 50 marks for oral presentation. A student should secure minimum 50% of marks for successful completion. In case, if a student fails, he/she shall reappear as and when semester supplementary examinations are conducted by the University.

13 Comprehensive Viva

A Comprehensive Viva shall be conducted after the II Semester examinations for 100 marks by a committee consisting of the Head of the Department, one senior faculty member of the same specialization, and an external subject expert appointed by the University. The student must secure a minimum of 50% marks to be declared as passed

14 Credits for Co-curricular Activities

The credits assigned for co-curricular activities shall be given by the principals of the colleges and the same shall be submitted to the University. A Student should earn 01 credits under the head of co-curricular activities, viz., attending Conference, Scientific Presentations and Other Scholarly Activities.

Following are the guidelines for awarding Credits for Co-curricular Activities

Name of the Activity	Maximum Credits / Activity
Participation in National Level Seminar/ Conference / Workshop /Training programs (related to the specialization of the student)	0.5

Participation in International Level Seminar / Conference / workshop/Training programs held outside India (related to the specialization of the student)	1
Academic Award/Research Award from State Level/National Agencies	0.5
Academic Award/Research Award from International Agencies	1
Research / Review Publication in National Journals (Indexed in Scopus / Web of Science)	0.5
Research / Review Publication in International Journals with Editorial board outside India (Indexed in Scopus / Web of Science)	1

Note:

i) Credit shall be awarded only for the first author. Certificate of attendance and participation in a Conference/Seminar is to be submitted for awarding credit. A minimum participation of five days is required to earn the necessary credits. Alternatively, the student may attend five different one day programs to meet this requirement.

ii) Certificate of attendance and participation in workshops and training programs (Internal or External) is to be submitted for awarding credit. The total duration should be at least one week.

iii) Participation in any activity shall be permitted only once for acquiring required credits under cocurricular activities

15 Grading:

As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades and corresponding percentage of marks shall be followed:

After each course is evaluated for 100 marks, the marks obtained in each course will be converted to a corresponding letter grade as given below, depending on the range in which the marks obtained by the student fall.

Structure of Grading of Academic Performance

Letter Grade	Marks Range	Grade Point
S	91-100	10
A	81-90	9
B	70-80	8
C	60-69	7
D	55-59	6
E	50-54	5
F	<50	0
Absent	Ab (Absent)	0

i) A student obtaining Grade 'F' or Grade 'Ab' in a subject shall be considered failed and will be required to reappear for that subject when it is offered the next supplementary examination.

ii) For noncredit audit courses, "Satisfactory" or "Unsatisfactory" shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA/Percentage.

Computation of Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.,

$$SGPA = \Sigma (C_i \times G_i)/\Sigma C_i$$

where, C_i is the number of credits of the i^{th} subject and G_i is the grade point scored by the student in the i^{th} course.

i) The Cumulative Grade Point Average (CGPA) will be computed in the same manner considering all the courses undergone by a student over all the semesters of a program, i.e.,

$$CGPA = \Sigma (C_i \times S_i) / \Sigma C_i$$

where "S_i" is the SGPA of the i^{th} semester and C_i is the total number of credits up to that semester.

ii) Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.

iii) While computing the SGPA the subjects in which the student is awarded Zero grade points will also be included.

Grade Point: It is a numerical weight allotted to each letter grade on a 10-point scale. Letter Grade: It is an index of the performance of students in a said course. Grades are denoted by letters S, A, B, C, D and F.

16 Award of Class:

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes:

Class Awarded	Percentage of Marks to be secured
First Class with Distinction	>=8
First Class	>= 7 and < 8
Pass Class	>=5 and < 7

17 Exit Policy:

The student shall be permitted to exit with a PG Diploma based on his/her request to the university through the respective institution at the end of first year subject to passing all the courses in first year.

The University shall resolve any issues that may arise in the implementation of this policy from time to time and shall review the policy in the light of periodic changes brought by UGC, AICTE and State government.

18 Withholding of Results:

If the candidate has any case of in-discipline pending against him/her, the result of the candidate shall be withheld, and he/she will not be allowed/promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

19 Transitory Regulations

Discontinued, detained, or failed candidates are eligible for readmission as and when the semester is offered after fulfillment of academic regulations. Candidates who have been detained for want of attendance or not fulfilled academic requirements or who have failed after having undergone the course in earlier regulations or have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to Section 2 and they will follow the academic regulations into which they are readmitted.

20 General:

20.1 The academic regulations should be read as a whole for purpose of any interpretation.

20.2 Disciplinary action for Malpractice/improper conduct in examinations is appended.

20.3 Where the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

20.4 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.

20.5 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the University.

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RULES FOR

DISCIPLINARY ACTION FOR MALPRACTICES / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	**Punishment**
	If the candidate:	
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred for four consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in

		connection with forfeiture of seat. The performance of the original candidate, who has been impersonated, shall be cancelled in all the subjects of the examination (including practical's and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for four consecutive semesters from class work and all University examinations if his involvement is established. Otherwise, the candidate is debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject only.
6.	Refuses to obey the orders of the Chief Superintendent /Assistant - Superintendent /any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. If the candidate physically assaults the invigilator/ officer-in-charge of the Examinations, then the candidate is also debarred and forfeits his/her seat. In case of outsiders, they will be handed over to the police and a police case is registered against them.

	or has the tendency to disrupt the orderly conduct of the examination.	
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject only or in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations, depending on the recommendation of the committee.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

1. Malpractices identified by squad or special invigilators
2. Punishments to the candidates as per the above guidelines.
3. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
4. A show cause notice shall be issued to the college.
5. Impose a suitable fine on the college.
6. Shifting the examination center from the college to another college for a specific period of not less than one year.

Note:

Whenever the performance of a student is cancelled in any subject/subjects due to Malpractice, he has to register for End Examinations in that subject/subjects consequently and has to fulfill all the norms required for the award of Degree.

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G. Pullaiah College of Engineering and Technology

(Autonomous)

(Approved by AICTE | NAAC Accreditation with 'A' Grade | Accredited by NBA (ECE & EEE) | Affiliated to JNTUA)

Nandikotkur Road, Venkayapalli (V), Kurnool – 518452, Andhra Pradesh

M.TECH IN DIGITAL ELECTRONICS & COMMUNICATION SYSTEMS

COURSE STRUCTURE & SYLLABI

SEMESTER – I

S.No.	Course codes	Course Name	Category	Hours per week			Credits	Scheme of Examination Maximum Marks		
				L	T	P	C	Internal	External	Total
1	C43801	Advanced Digital System Design	PC	3	0	0	3	40	60	100
2	C43802	Wireless Communication and Networks	PC	3	0	0	3	40	60	100
3	C43803a C43803b C43803c	**Program Elective – I** Design for Testability VLSI Technology and Design SoC Architecture	PE	3	0	0	3	40	60	100
4	C43804a C43804b C43804c	**Program Elective – II** Software Defined Radio Optical Communication and Networks 5G Communications	PE	3	0	0	3	40	60	100
5	C43805	Advanced Digital System Design Lab	PC	0	0	4	2	40	60	100
6	C43806	Wireless Communication and Networks	PC	0	0	4	2	40	60	100
7	C43807	Research Methodology and IPR	MC	2	0	0	2	40	60	100
8	C43808	RTL Synthesis, Simulation and Verification	SE	0	1	2	2	40	60	100
9	C43809	**Audit Course – I**	AC	2	0	0	0	40*	-	40*
Total							20	320	480	800

*There is no external examination for audit course. Student shall be declared to have passed the mandatory course only when he/she secures 50% or more in the internal examinations.

SEMESTER – II

S.No.	Course codes	Course Name	Category	Hours per week			Credits	Scheme of Examination		
				L	T	P		Internal	External	Total
1.	C43810	Network Security and Cryptography	PC	3	0	0	3	40	60	100
2.	C43811	Advanced Communications and Networks	PC	3	0	0	3	40	60	100
3.	C43812a C43812b C43812c	**Program Elective – III** Embedded Real Time Operating Systems Communication Buses and Interfaces Embedded Systems Protocols	PE	3	0	0	3	40	60	100
4.	C43813a C43813b C43813c	**Program Elective – IV** Cognitive Radio Image and Video Processing Ad hoc and Wireless Sensor Networks	PE	3	0	0	3	40	60	100
5.	C43814	Network Security and Cryptography Lab	PC	0	0	4	2	40	60	100
6.	C43815	Advanced Communications and Networks Lab	PC	0	0	4	2	40	60	100
7.	C43816	Quantum Technologies and Applications	MC	2	0	0	2	40	60	100
8.	C43817	Comprehensive Viva Voce	PC	0	0	0	2	100	-	100
9.	C43818	**Audit Course – II**	AC	2	0	0	0	40*	-	-
Total							20	380	420	800

*There is no external examination for audit course. Student shall be declared to have passed the mandatory course only when he/she secures 50% or more in the internal examinations.

SEMESTER – III

S.No.	Course codes	Course Name	Category	Hours per week			Credits	Scheme of Examination Maximum Marks		
				L	T	P		Internal	External	Total
1.	C43819a C43819b C43819c	**Program Elective – V** Voice and Data Networks Industrial Internet of Things Artificial Intelligence and Machine Learning	PE	3	0	0	3	40	60	100
2.	C43820	**Open Elective -I** IoT and its Applications	OE	3	0	0	3	40	60	100
3.	C43821	Dissertation Phase – I	PR	0	0	20	10	100	-	100
	C43822	Industry Internship		0	0	0	2	100	-	100
4.	C43823	Co-curricular Activities		0	0	0	1	Grade		
Total							**19**	**280**	**120**	**400**

SEMESTER - IV

S.No.	Course codes	Course Name	Category	Hours per week			Credits	Scheme of Examination		
				L	T	P		Internal	External	Total
1.	C43824	Dissertation Phase – II	PR	0	0	32	16	100	100	200
Total							**16**	**100**	**100**	**200**

Course Code	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	C
C43801		3	0	0	3
	Semester		**I**		

Course Objectives:

- To understand an overview of system design approach using programmable logic devices.
- To implement combinational logic circuit design.
- To implement sequential logic circuit design.
- To learn software tools used for design process with the help of case studies.

Course Outcomes (CO): Student will be able to

- Understand an overview of system design approach using programmable logic devices.
- Implement combinational logic circuit design.
- Implement sequential logic circuit design.
- Learn software tools used for design process with the help of case studies.

UNIT - I		Lecture Hrs:

Processor Arithmetic: Two's Complement Number System - Arithmetic Operations; Fixed point Number System; Floating Point Number system - IEEE 754 format, Basic binary codes.

UNIT - II		Lecture Hrs:

Combinational circuits: CMOS logic design, Static and dynamic analysis of Combinational circuits, timing hazards. Functional blocks: Decoders, Encoders, Three-state devices, Multiplexers, Parity circuits, Comparators, Adders, Subtractors, Carry look-ahead adder – timing analysis. Combinational multiplier structures.

UNIT - III		Lecture Hrs:

Sequential Logic - Latches and Flip-Flops, Sequential logic circuits - timing analysis (Set up and hold times), State machines - Mealy & Moore machines, Analysis, FSM design using D Flip-Flops, FSM optimization and partitioning; Synchronizers and metastability. FSM Design examples: Vending machine, Traffic light controller, Washing machine.

UNIT - IV		Lecture Hrs:

Subsystem Design using Functional Blocks (1) - Design (including Timing Analysis) of different logical blocks of varying complexities involving mostly combinational circuits: ALU, 4-bit combinational multiplier, Barrel shifter, Simple fixed point to floating point encoder, Dual Priority encoder, Cascading comparators

UNIT - V		Lecture Hrs:

Subsystem Design using Functional Blocks (2) - Design, (including Timing Analysis) of different logical blocks of different complexities involving mostly sequential circuits: Pattern (sequence) detector, Programmable Up-down counter, Round robin arbiter with 3 requesters, Process Controller, FIFO

Textbooks:

1. M. Morris Mano, Michael D. Ciletti, "Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog", Pearson Education; 6th Edition, 2018
2. John F. Wakerly, "Digital Design", Prentice Hall, 3rd Edition, 2002.

Reference Books:

1. Digital Circuits and Logic Design-Samuel C.LEE, PHI, 2008.
2. Digital System Design using programmable logic devices- Parag K. Lala, BS publications.

Course Code	WIRELESS COMMUNICATIONS AND NETWORKS	L	T	P	C
C43802		3	0	0	3
	Semester	I			

Course Objectives:

- To study the Channel planning for Wireless Systems
- To study the Mobile Radio Propagation
- To study the Equalization and Diversity
- To study the Wireless Networks

Course Outcomes (CO):

- Understand Cellular communication concepts
- Study the mobile radio propagation
- Study the wireless network different type of MAC protocols

UNIT - I		Lecture Hrs:

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference, Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring.

UNIT - II		Lecture Hrs:

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction-Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models-Longley-Ryce Model, Okumura Model, Hata Model, PCS Extension to Hata Model, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

UNIT - III		Lecture Hrs:

Mobile Radio Propagation: Small –Scale Fading and Multipath: Small Scale Multipath propagation Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT - IV		Lecture Hrs:

Equalization and Diversity: Introduction, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non-linear Equalization-Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm. Diversity Techniques-Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal

Gain Combining, Polarization Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.		
UNIT - V		Lecture Hrs:
Wireless Networks: Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11, IEEE 802.11 Medium Access Control, Comparison of IEEE 802.11 a, b, g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, Hiper Lan, WLL.		
Textbooks:		
1. Wireless Communications, Principles, Practice – Theodore, S. Rappaport, 2nd Ed., 2002, PHI. 2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press. 3. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE 4. Mobile Cellular Communication – Gottapu Sasibhushana Rao, Pearson Education, 2012.		
Reference Books:		
1. Wireless Digital Communications – Kamilo Feher, 1999, PHI. 2. Wireless Communication and Networking – William Stallings, 2003, PHI		

Course Code	DESIGN FOR TESTABILITY	L	T	P	C
C43803a	Program Elective – I	3	0	0	3
	Semester	I			

Course Objectives:

- To introduce the fundamental concepts, types, and philosophies of VLSI testing.
- To familiarize fault models and apply logic/fault simulation techniques for test evaluation.
- To study testability measures and design-for-test (DFT) techniques including scan design.
- To explore Built-In Self-Test (BIST) strategies and their application in digital systems.
- To learn the boundary scan architecture and standards used in board-level testing.

Course Outcomes (CO): Student will be able to

- Explain the role of testing in VLSI systems and differentiate between fault models and testing types.
- Apply simulation algorithms for design verification and fault analysis in digital circuits.
- Evaluate testability using measures like SCOAP and design scan-based test structures.
- Design and implement BIST strategies for logic and memory testing.
- Demonstrate understanding of boundary scan standards and describe systems using BSDL.

UNIT - I		Lecture Hrs:

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modelling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II		Lecture Hrs:

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modelling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT - III		Lecture Hrs:

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT - IV		Lecture Hrs:

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per- Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V		Lecture Hrs:

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Textbooks:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Publishers.
2. VLSI Test Principles and Architectures: Design for Testability" – L.-T. Wang, C.-W. Wu, X. Wen

Reference Books:

1. Digital Systems and Testable Design - M. Abramovici, M. A. Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

Course Code	VLSI TECHNOLOGY AND DESIGN	L	T	P	C
C43803b	Program Elective – I	3	0	0	3
	Semester	I			

Course Objectives:

- To familiarize with large scale integration technology.
- To expose fabrication methods, layout and design rules.
- To learn methods to improve Digital VLSI system's performance.
- To know about VLSI Design constraints.

Course Outcomes (CO):

- Familiarize with large scale integration technology.
- Expose fabrication methods, layout and design rules.
- Learn methods to improve Digital VLSI system's performance.
- Know about VLSI Design constraints.

UNIT - I — Lecture Hrs:

Review of Microelectronics and Introduction to MOS Technologies- MOS, CMOS, Bi CMOS Technology. Basic Electrical Properties of MOS, CMOS &Bi CMOS Circuits: Ids – Vds relationships, Threshold Voltage V_T, g_m, g_{ds} and ω_o, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT - II — Lecture Hrs:

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.
Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT - III — Lecture Hrs:

Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT - IV — Lecture Hrs:

Sequential Systems: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT – V — Lecture Hrs:

Floor Planning: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

Textbooks:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2010
2. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
3. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

Course Code	SoC ARCHITECTURE	L	T	P	C
C43803c	Program Elective – I	3	0	0	3
	Semester	I			

Course Objectives:

- To understand the basics related to SoC architecture and different approaches related to SoC Design.
- To select an appropriate robust processor for SoC Design
- To select an appropriate memory for SoC Design.
- To realize real time case studies

Course Outcomes (CO): Student will be able to

- Understand the basics related to SoC architecture and different approaches related to SoC Design.
- Select an appropriated robust processor for SoC Design
- Select an appropriate memory for SoC Design.
- Realize real time case studies

UNIT - I Lecture Hrs:

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory &Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT - II Lecture Hrs:

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors

UNIT - III Lecture Hrs:

Memory Design for SOC: Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT - IV Lecture Hrs:

Interconnect, Customization and Configurability: Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT - V Lecture Hrs:

Application Studies / Case Studies: SOC Design approach; AES-algorithms, Design and evaluation; Image compression–JPEG compression.

Textbooks:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber, 2ndEdition, 2000, Addison Wesley Professional.

Reference Books:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2.Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3.System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers

Course Code	SOFTWARE DEFINED RADIO	L	T	P	C
C43804a	Program Elective – II	3	0	0	3
	Semester	I			

Course Objectives:

- Introduce the evolution of radio communication systems and the fundamental concepts, architectures, and design principles of Software Defined Radio (SDR).
- Understand the implementation challenges in RF front-end systems, including dynamic range, receiver topologies, and performance-affecting factors.
- Explore digital signal generation techniques, particularly direct digital synthesis (DDS), and analyze related spurious signal behaviors.
- Introduce multi rate signal processing methods such as sample rate conversion, polyphase filters, and timing recovery in digital receivers.
- Study analog-to-digital and digital-to-analog conversion techniques and methods for improving data converter performance in SDR systems.

Course Outcomes (CO):

Upon completion of the course students will be able to:

- Know the fundamentals of Software Radios, their evolution from traditional radios, and various levels including SCR, SDR, ISR, and USR.
- Analyse RF front-end architectures, dynamic range requirements, and the role of RF Components in system performance for Software Radio implementation.
- Explain and compare different signal generation techniques including direct digital synthesis, and analyse sources of spurious components and jitter effects.
- Apply multi-rate signal processing techniques such as sample rate conversion, polyphase Filtering, and digital filter banks in software radio systems.
- Evaluate the performance of A/D and D/A converters in practical systems, and describe Methods to improve conversion performance, including relevance to JTRS

UNIT - I		Lecture Hrs:

Introduction to Software radio concepts: Introduction, need, characteristics, benefits and design principles of Software Radios. Traditional radio implemented in hardware (first generations of 2G cell phones), Software controlled radio (SCR), Software defined radio (SDR), Ideal software radio (ISR), Ultimate software radio (USR)

UNIT - II		Lecture Hrs:

Radio frequency implementation issues: The purpose of RF Front-End, Dynamic range, RF Receiver Front-End Topologies, Enhanced Flexibility of the RF Chain with Software Radios, Importance of Components to Overall performance, Transmitter Architecture and their issues, Noise and Distortion in RF Chain.

UNIT - III		Lecture Hrs:

Digital generation of signals: Introduction, Comparison of Direct Digital Synthesis with Analog Signal Synthesis, Approaches to Direct Digital Synthesis, Analysis of Spurious Signals, Spurious components due to Periodic Jitter.

UNIT - IV		Lecture Hrs:

Multi rate Signal Processing: Introduction, Sample Rate Conversion Principles, Polyphase Filters, Digital Filter Banks, Timing Recovery in Digital receivers Using Multi rate Digital Filters.

UNIT - V		Lecture Hrs:

A/D & D/A Conversion: Introduction, Parameters of Ideal Data Converters, Parameters of Practical data Converters, Techniques to improve Data Converter performance, JTRS.

Textbooks:

1. Jeffery H. Reed, “Software Radio, (A modern approach to radio engineering)”, PHI PTR, 2002
2. John J. Rouphael, “RF and Digital Signal Processing for Software Defined Radio” Elsevier,

Newness Publications.
Reference Books:
1. C. Richard Johnson, Jr., and William A. Sethares, Telecommunication Breakdown, Prentice Hall, ISBN 0-13-143047-5, 2004 2. Software Defined Radio: Theory and Practice by John M. Reyland (Artech House, 2023)

Course Code	OPTICAL COMMUNICATIONS AND NETWORKS	L	T	P	C
C43804b	Program Elective – II	3	0	0	3
	Semester	I			

Course Objectives:

- To understand the concept and structures of optical fibers.
- To study about the photo sources and detectors in digital and analog domains.
- To learn various network topologies and protocols
- To study about performance measurement and monitoring of optical communication systems.

Course Outcomes (CO):

- Understand the concept and structures of optical fibers.
- Study about the photo sources and detectors in digital and analog domains.
- Learn various network topologies and protocols
- Study about performance measurement and monitoring of optical communication systems.

UNIT - I		Lecture Hrs:

Optical Fibers: Structures, waveguiding and Fabrication: Nature of Light, Basic optical laws and definitions, Single mode fibers, Graded index fiber structure, Attenuation, Signal Dispersion in fibers.
Optical Sources- LEDs, Laser Diodes, Line Coding.

UNIT - II		Lecture Hrs:

Photo detectors: Photo detector Noise, Detector Response Time, Avalanche Multiplication Noise.
Optical Receiver Operation: Fundamental receiver operation, Digital receiver performance, Eye diagrams.
WDM Concepts and Components: Passive optical Couplers, Isolators and Circulators

UNIT - III		Lecture Hrs:

Digital Links: Point to point links, power penalties, error control, Coherent detection, Differential Quadrature Phase Shift Keying.
Analog Links: Carrier to noise ration, Multichannel Transmission Techniques, RF over Fiber, Radio over fiber links, Microwave Photonics.

UNIT - IV		Lecture Hrs:

Optical Networks: Network Concepts, Network Topologies, SONET/SDH, High speed light wave links, Optical add/ Drop Multiplexing, Optical Switching, WDM Network, Passive Optical Networks, IP Over DWDM, Optical Ethernet, Mitigation of Transmission Impairments

UNIT - V		Lecture Hrs:

Performance Measurement and Monitoring: Measurement standards, Basic Test Equipment, Optical power measurement, Optical fiber characterization, Eye diagram tests, optical time domain reflectometer, optical performance monitoring, optical fiber system performance measurements.

Textbooks:

1. Gerd Keiser, “Optical Fiber Communications”, 5th Edition, Mc Graw Hill.
2. Rajeev Ramaswamy and Kumar N Sivarajan, “Optical Networks: A Practical Perspective”, 2nd Ed., 2004, Elsevier Morgan Kaufmann Publishers (An imprint of Elsevier).

Reference Books:

1. John. M. Senior, “Optical Fiber Communications: Principles and Practice”, 2nd Ed, 2000, PE.
2. Harold Kolimbris, “Fiber Optic Communication”, 2nd Ed, 2004, PEI
3. Uyless Black, “Optical Networks: Third Generation Transport Systems”, 2nd Ed, 2009, PEI
4. Govind Agarwal, “Optical Fiber Communications”, 2nd Ed, 2004, TMH.
5. S. C. Gupta, “Optical Fiber Communications and its Applications”, 2004, PH

Course Code	5G COMMUNICATIONS	L	T	P	C
C43804c	Program Elective – II	3	0	0	3
	Semester	I			

Course Objectives:

- To understand 5G Technology advances and their benefits
- To learn the key RF, PHY, MAC and air interface changes required to support 5G
- To acquire knowledge on Device-to-device communication and millimeter wave communication
- To explore implementation options for 5G

Course Outcomes (CO):

- Understand 5G Technology advances and their benefits
- Learn the key RF, PHY, MAC and air interface changes required to support 5G
- Acquire knowledge on Device-to-device communication and millimeter wave communication
- Explore implementation options for 5G

UNIT - I		Lecture Hrs:

Overview of 5G Broadband Wireless Communications:
Evolution of mobile technologies 1G to 4G (LTE, LTEA, LTEA Pro), An Overview of 5G requirements, Regulations for 5G, Spectrum Analysis and Sharing for 5G.

UNIT - II		Lecture Hrs:

The 5G wireless Propagation Channels:
Channel modeling requirements, propagation scenarios and challenges in the 5G modeling, Channel Models for mm Wave MIMO Systems.

UNIT - III		Lecture Hrs:

Transmission and Design Techniques for 5G:
Basic requirements of transmission over 5G, Modulation Techniques – Orthogonal frequency division multiplexing (OFDM), generalized frequency division multiplexing (GFDM), filter bank multi-carriers (FBMC) and universal filtered multi-carrier (UFMC), Multiple Accesses Techniques – orthogonal frequency division multiple accesses (OFDMA), generalized frequency division multiple accesses (GFDMA), nonorthogonal multiple accesses (NOMA).

UNIT - IV		Lecture Hrs:

Device-to-Device (D2D) and Machine-to-Machine (M2M) type Communications
Extension of 4G D2D standardization to 5G, radio resource management for mobile broadband D2D, multi-hop and multi-operator D2D communications.

UNIT - V		Lecture Hrs:

Millimeter-wave Communications
Spectrum regulations, deployment scenarios, beamforming, physical layer techniques, interference and mobility management, Massive MIMO propagation channel models, Channel Estimation in Massive MIMO, Massive MIMO with Imperfect CSI, Multi-Cell Massive MIMO, Pilot Contamination, Spatial Modulation (SM).

Textbooks:

1. Martin Sauter “From GSM From GSM to LTE–Advanced Pro and 5G: An Introduction to Mobile Networks and Mobile Broadband”, Wiley-Blackwell.
2. Afif Osseiran, Jose. F. Monserrat, Patrick Marsch, “Fundamentals of 5G Mobile Networks”, Cambridge University Press.
3. Athanasios G. Kanatos, Konstantina S. Nikita, Panagiotis Mathiopoulos, “New Directions in Wireless Communication Systems from Mobile to 5G”, CRC Press.
4. Theodore S. Rappaport, Robert W. Heath, Robert C. Danials, James N. Murdock “Millimeter Wave Wireless Communications”, Prentice Hall Communications.

Reference Books:

1. Jonathan Rodriguez, “Fundamentals of 5G Mobile Networks”, John Wiley & Sons.
2. Amitabha Ghosh and Rapeepat Ratasuk “Essentials of LTE and LTE-A”, Cambridge University Pres

Course Code	ADVANCED DIGITAL SYSTEM DESIGN LAB	L	T	P	C
C43805		0	0	4	2
Semester		I			

Course Objectives:

- To familiarize the HDL simulator / synthesis tool
- To design and implement given combinational circuit on FPGA device
- To design and implement given sequential circuit on FPGA device

Course Outcomes (CO):

- Familiarize the HDL simulator / synthesis tool
- Design and implement given combinational circuit on FPGA device
- Design and implement given sequential circuit on FPGA device

List of Experiments:

Student has to design ANY TWELVE experiments of his/her user defined library components by using and standard HDL simulator / Synthesis tool for target FPGA device.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry
3. Look Ahead Adder.
4. Design of 2-to-4 decoder
5. Design of 8-to-3 encoder (without and with parity)
6. Design of 8-to-1 multiplexer
7. Design of 4 bit binary to gray converter
8. Design of Multiplexer/ Demultiplexer, comparator
9. Design of Full adder using 3 modeling styles
10. Design of flip flops: SR, D, JK, T
11. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
12. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in
13. Serial out and Parallel in Parallel Out.
14. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
15. Design of 4- Bit Multiplier, Divider.
16. Design of ALU to Perform – ADD, SUB, AND-OR, 1’s and 2’s Compliment,
17. Multiplication, and Division.
18. Design of Finite State Machine.
19. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.

Course Code	WIRELESS COMMUNICATIONS AND NETWORKS LAB	L	T	P	C
C43806		0	0	4	2
Semester		I			

Course Objectives:

- To understand concepts of GSM/CDMA technologies
- To implement signal processing algorithms for the given specifications
- To implement wireless communication algorithms for the given specifications

Course Outcomes (CO):

- Understand concepts of GSM/CDMA technologies
- Implement signal processing algorithms for the given specifications
- Implement wireless communication algorithms for the given specifications

List of Experiments:

Student has to design ANY TWELVE experiments.

1. Implementation of Convolutional Encoder and Decoder.
2. Simulation of the following Outdoor Path loss propagation models using MATLAB.
a. Free Space Propagation model
b. Okumura model
c. Hata model
3. Simulation of Adaptive Linear Equalizer using MAT LAB software.
4. Measurement of call blocking probability for GSM &CDMA networks using NetSim software.
5. Study of GSM handset for various signaling and fault insertion techniques (Major GSM handset sections: clock, SIM card, charging, LCD module, Keyboard, User interface).
6. Study of transmitter and receiver section in mobile handset and measure frequency
7. Baseband signal and GMSK modulating signal.
8. Simulation of RAKE Receiver for CDMA communication using MAT LAB software.
9. Simulate and test various types of PN codes, chip rate, spreading factor and processing gain on performance of DSSS in CDMA.
10. Simulate and test the 3G Network system features using GSM AT Commands. (Features of 3G Communication system: Transmission of voice, video calls, SMS, MMS, TCP/IP, HTTP, GPS)
11. Modelling of communication system using Simulink.
12. Simulate Least Mean Square Algorithm
13. Simulate Recursive least squares algorithm.
14. Observe Waveforms at various test points of a mobile phone using Mobile Phone Trainer

Course Code	RESEARCH METHODOLOGY AND IPR	L	T	P	C
C43807		2	0	0	2
	Semester	I			

Course Objectives:

- Identify an appropriate research problem in their interesting domain.
- Understand ethical issues understand the Preparation of a research project thesis report.
- Understand the Preparation of a research project thesis report
- Understand the law of patent and copyrights.
- Understand the Adequate knowledge on IPR

Course Outcomes (CO): Student will be able to

- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT - I		Lecture Hrs:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, scope, and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT - II		Lecture Hrs:

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT - III		Lecture Hrs:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT - IV		Lecture Hrs:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT - V		Lecture Hrs:

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Textbooks:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

Reference Books:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.

Course Code	RTL SYNTHESIS, SIMULATION AND VERIFICATION	L	T	P	C
C43808		0	1	2	2
Semester		I			

Course objectives: This course aims to

- The simulation of combinational and sequential circuits.
- FSM based designs.
- Implementation of DFT and FFTs.
- Verify layout of basic digital circuits.

Course outcomes: After completion of this course, students will be able to

1. Demonstrate the process steps required for simulation /synthesis.
2. Design and simulate various combinational and sequential circuits using HDL.
3. Develop an RTL code for various real time applications.
4. Synthesize / Simulate an RTL code for several digital designs
5. Build and verify various digital circuits.

Module 1 – Introduction to RTL Design

- RTL design flow: Specification → RTL coding → Synthesis → Simulation → Verification.
- HDL coding styles for synthesis (SystemVerilog/VHDL basics).
- Lab:
    1. Write synthesizable Verilog/SystemVerilog code for:
        a) Half Adder, Full Adder
        b) 4-bit Ripple Carry Adder
        c) 4-bit Synchronous Counter (Up/Down)
    2. FSM Design: Sequence Detector (e.g., detect “1011”).

Module 2 – RTL Synthesis

- Synthesis concepts: mapping RTL to gate-level netlist.
- Constraints: clock, area, power.
- Lab:
    1. Synthesize combinational and sequential circuits (Adder, Counter, FSM) using EDA tool
    2. Generate gate-level netlist and analyze area, delay, power reports.
    3. Apply constraints (clock, timing) and observe impact on synthesis results.

Module **3 – Simulation**

- Functional vs. Timing simulation.
- Testbench creation, waveforms, debugging.
- Lab: Run simulations
    1. Develop testbenches for:
    a) 4-bit ALU (add, sub, AND, OR).
    b) Universal Shift Register.
    2. Perform functional simulation using EDA tools
    3. Perform post-synthesis (timing) simulation and compare results with functional simulation.

Module 4 – Verification

- Verification basics: functional verification, assertion-based verification.
- Introduction to UVM/OVM concepts.
- Lab: Writing simple verification testbenches.
    1. Write self-checking testbenches for combinational and sequential circuits.
    2. Use assertion-based verification (SystemVerilog Assertions – SVA) for protocol checks (e.g., handshaking signals).
    3. Coverage-driven verification experiment: Create random test cases for FIFO/Memory.

Module 5 – Case Study & Mini Project

- Design, synthesize, and verify a digital subsystem (e.g., ALU, UART, FIFO).
- End-to-end RTL → Synthesis → Simulation → Verification flow.
- Lab: Design, synthesize, simulate, and verify a **digital subsystem** such as:

    1. UART Transmitter/Receiver
    2. Simple CPU Core Module (Instruction Decoder + ALU + Register File)
    3. FIFO Buffer with full/empty flags

Textbooks / References

1. Samir Palnitkar – *Verilog HDL: A Guide to Digital Design and Synthesis*.
2. Michael Ciletti – *Advanced Digital Design with the Verilog HDL*.
3. Chris Spear & Greg Tumbush – *SystemVerilog for Verification*.
4. David Rich – *Design and Verification with SystemVerilog*.

Suggested reading:

1. Samir Palnitkar, "Verilog HDL, a guide to digital design and synthesis", Prentice Hall 2003.
2. Doug Amos, Austin Lesea, Rene Richter, "FPGA based prototyping methodology manual", Xilinx, 2011.
3. Bob Zeidman, "Designing with FPGAs & CPLDs", CMP Books, 2002.